V-Band Integrated Quadriphase Modulator

Final Report

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FOREWORD

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Publication of this report does not constitute NASA approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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1. INTRODUCTION

The objective of this program was to develop a V-band integrated circuit quadriphase shift keyed (QPSK) modulator/exciter for space communications systems. Future intersatellite communications systems will require direct modulation at 60 GHz to enhance the signal processing capability. For most systems, particularly space applications, small and lightweight components are essential to alleviate severe system design constraints. Thus, to achieve wide-band, high data rate systems, direct modulation techniques at millimeter waves using solid-state integrated circuit technology are an integral part of the overall technology developments.

Recognizing the need for high data rate communication systems, TRW has been actively engaged in the research and development of advanced integrated circuit modulators and receivers for the past several years. Integrated circuit receivers have been developed using solid-state and MIC technologies at Ka- and V-band. In the area of modulator developments, we have demonstrated a Ku-band and V-band QPSK modulator under NASA contracts (NAS5-25354 and NAS5-26223).

The development goal of this program was to extend the existing technologies for the development of a V-band modulator/exciter subsystem to establish a small lightweight brassboard model. Emphasis was placed on small size and high performance.

Figure 1-1 shows the modulator/exciter functional block diagram. The design goals and actual performance are presented in Table 1-1. The majority of the design goals were achieved.

The development effort was divided into four major areas: exciter development, modulator development, data driver development, and exciter/modulator integration and testing.

In the exciter development, a phaselocked Gunn oscillator has been developed with over +11 dBm output power. The oscillator has a locking range of 350 MHz and capture range of ±10 MHz.

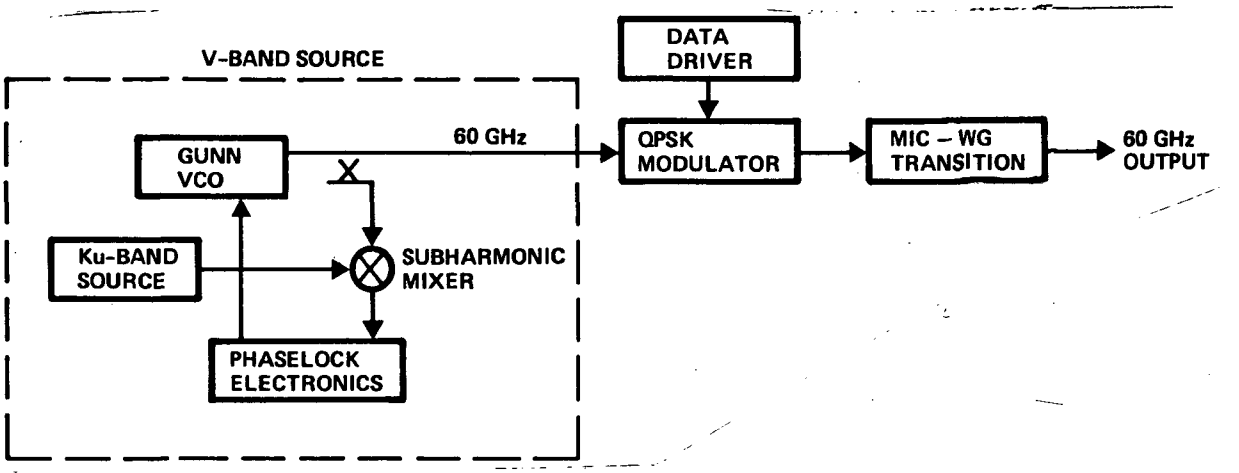


Figure 1-1. Functional Block Diagram

TABLE 1-1. Summary of Design Goals and Actual Performance

Specifications	Design Goals	Actual Performance
Carrier Frequency	60 GHz nominal	60 GHz
Modulation Format	QPSK	QPSK
Data Rate	2 Gbits per channel	Tested up to 650 MBPS
Maximum Amplitude Error	±0.5 dB	±0.5 dB
Maximum Phase Error	±3 deg	±3 deg
Data Transition Time	< 650 psec	650 psec
Data Asymmetry	< 5%	-
Exciter Stability	0.1 ppm per 24 hours	±30 ppm over -25 to 60°C
Modulated Power Output	0 dBm minimum	-2 dBm
Size	< 4 $in.^3$	4.05 $in.^3$ *
Weight	< 0.5 lb.	0.3 lb*
Power Consumption	< 15 W	22 W **

*For exciter/modulator module and data driver module only.

**Three power supplies are required: +15 V, 662 mA; -12 V, 485 mA; and +6.5 V, 980 mA. The total power consumption is 22 W. This power includes 3.28 W dissipated in the regulation process.

In the modulator development, a QPSK modulator was developed using a combination of microstrip and slotline transmission media built on sapphire substrate. The best results are 13 dB insertion loss, ±3° phase error, and ±0.5 dB amplitude error. The data rise time is about 650 psec.

In the data driver development, a high data rate driver has been constructed. The unit was hybridized into a small package measuring 1.8 x 2.5 x 0.55 in. The data driver was tested and operated up to 650 MBPS.

In the integration and testing, the exciter/modulator was integrated with the data driver into a small housing measuring 1.8 x 2.5 x 0.9 in. The modulator was fully characterized. Measurements included power output, return loss, static phase and amplitude error, modulated spectrum, rise time, eye pattern, and bit error rate (BER).

This report comprises seven sections: Section 2 describes the phase-locked exciter development; Section 3 presents the QPSK modulator development; Section 4 presents the data driver development and tests; Section 5 describes the integration and packaging; Section 6 presents the electrical and RF tests; Section 7 presents conclusions and recommendations for future study.

2. EXCITER DEVELOPMENT

The 60 GHz exciter consists of a Gunn VCO phaselocked to a low frequency reference source to achieve high stability and low FM noise. This section describes the development of the MIC Gunn VCO, subharmonic mixer, Ku-band reference source, and phaselock electronics. A block diagram of the exciter is shown in Figure 2-1.

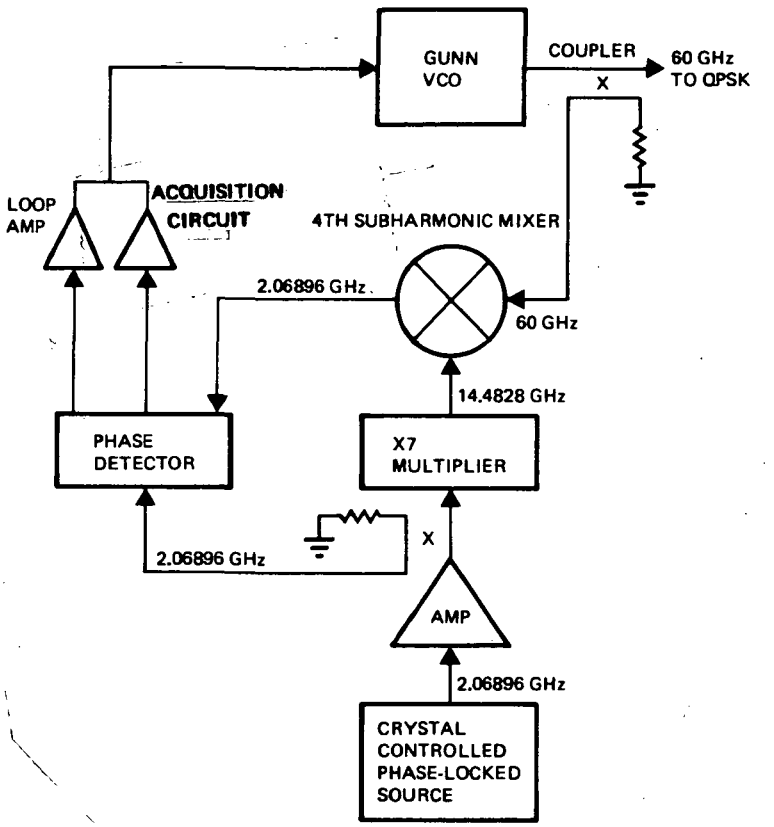


Figure 2-1. 60 GHz Phaselocked Gunn VCO

2.1 MIC GUNN VCO

In the oscillator design, one of the crucial parameters is the characterization of the Gunn diode. It is well known for a negative resistance oscillator that oscillation can occur whenever the real part of the Gunn device is greater than the external load resistance and the imaginary part of the circuit impedance is a conjugate match to that of the device. Aside

from the basic frequency range over which the Gunn device may be operated, the tuning range of a varactor-tuned Gunn oscillator is also governed by the circuit configuration, the varactor capacitance ratio, and circuit parasitics. To minimize circuit parasitics, chip devices should be employed whenever possible.

A chip varactor can easily be implemented in a microstrip circuit. Varactor chips with reasonable Q and capacitance ratio are easily obtainable. Figure 2-2 shows the typical C-V curve of a GaAs varactor chip. Although a chip Gunn diode is ideal in a wideband oscillator circuit design, there are many problems associated with this approach:

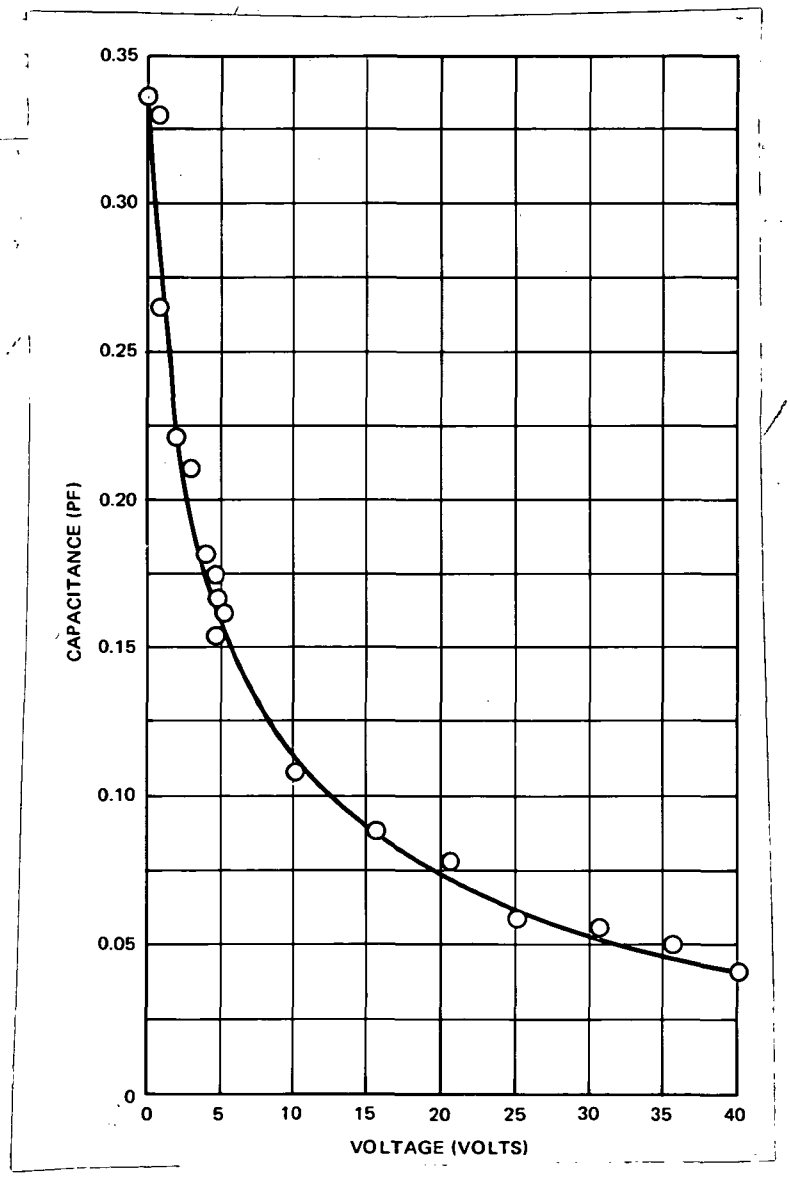


Figure 2-2. Tuning Varactor C-V Curve

- A chip device is difficult to test; therefore, assuring performance in an actual circuit application is a problem.
- Heat sinking may present problems in microstrip circuits.
- Chip devices are usually not reusable and this is important in the circuit optimization process.

We therefore used a packaged GaAs Gunn device, which was initially characterized in a waveguide cavity. A chip varactor was chosen as the tuning element.

From our analysis, a shunt-connected varactor gives the widest tuning range compared to a series-connected varactor. Figure 2-3 shows the equivalent circuit for a fixed tuned MIC Gunn oscillator. This equivalent circuit can be modified to include the varactor diode, as shown in Figure 2-4.

Characterization of the Gunn diode was accomplished using the equivalent circuit shown in Figure 2-3. Package parasitics are generally given by the manufacturer. For this circuit to oscillate, Im Zg = $-\text{Im } Z_T$ and Re/Zg/ $>$ Re Z_T, where Zg and Z_T are the Gunn diode and transformed load

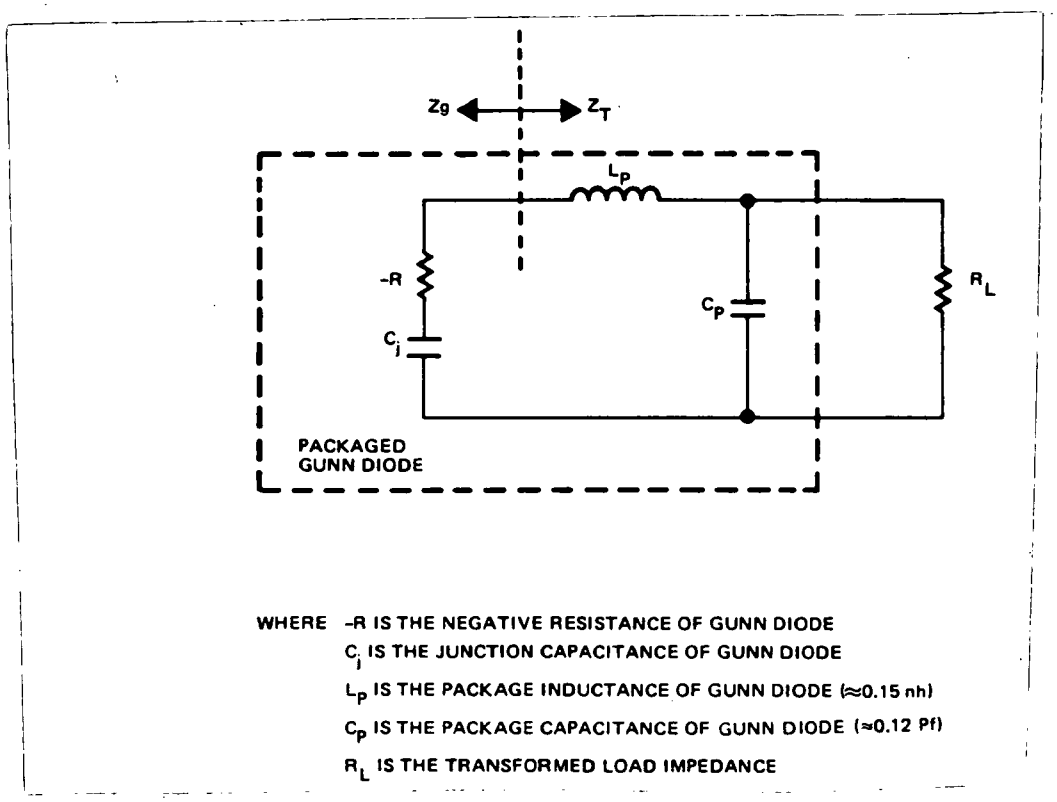


Figure 2-3. Fixed Tuned Gunn Oscillator Equivalent Circuit.

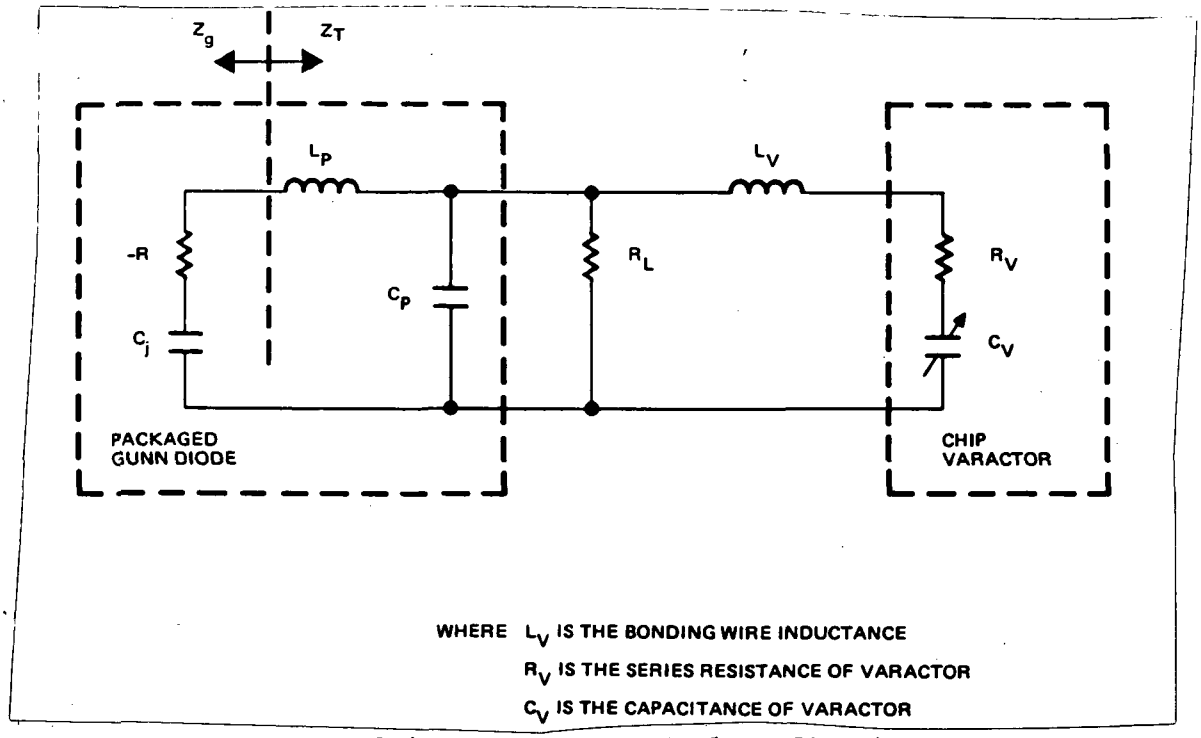


Figure 2-4. Gunn VCO Equivalent Circuit

impedance, respectively. A microstrip transformer was used to accomplish the impedance transformation. A simple circuit analysis showed that the transformed load impedance, Z_T, must be small to satisfy the condition $Re/Zg/ > Re\ Z_T$ ($Re/Zg/$ is generally around 8 ohms). This is demonstrated in Figure 2-5. For practical purposes, a load impedance of 250 ohms was chosen. By observing the oscillation frequency, C_j can be calculated by

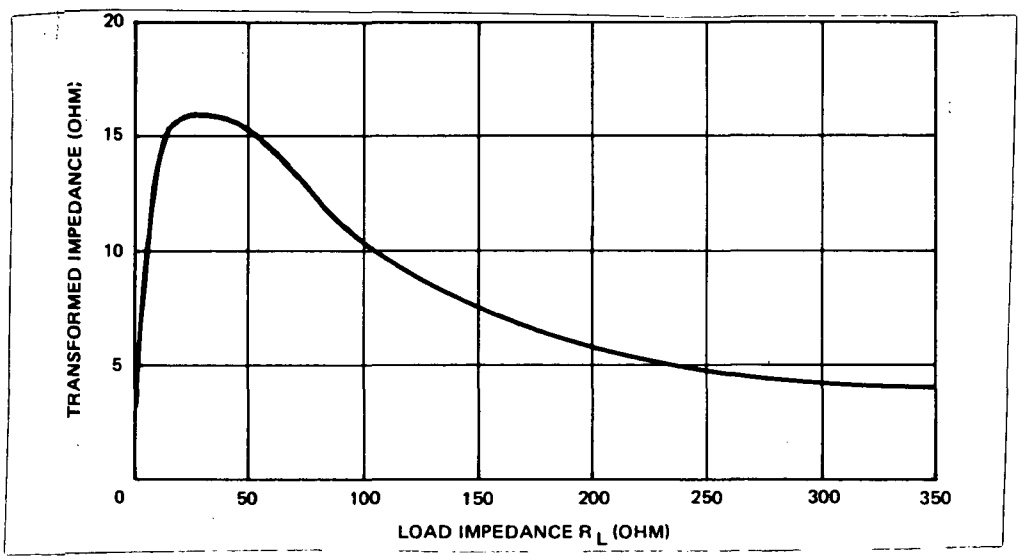


Figure 2-5. Transformed Impedance vs Load Impedance

$$C_j = \frac{1 + \omega^2 R_L^2 C_p^2}{\omega^2 \left(L_p - R_L^2 C_p + \omega^2 C_p^2 R_L^2 L_p \right)} \qquad (2.1\text{-}1)$$

Using the C_j calculated from Eq. (2.1-1) and the equivalent circuit of Figure 2-4, we can calculate Z_g and Z_T

$$Z_g = -R - j \frac{1}{\omega C_j} \qquad (2.1\text{-}2)$$

$$Z_T = j\omega L_p + \frac{R_L \left[R_V + j \left(\omega L_V - \frac{1}{\omega C_V} \right) \right]}{\left(R_L + R_V - \omega^2 R_L C_p L_V + \frac{R_L C_p}{C_V} \right) + j \left(\omega L_V - \frac{1}{\omega C_V} + \omega R_L R_V C_p \right)} \qquad (2.1\text{-}3)$$

The varactor tuning range can be computed by solving the following equation for different values of C_V:

$$\text{Im } Z_g = -\text{Im } Z_T \qquad (2.1\text{-}4)$$

A V-band MIC Gunn VCO operating at 57 GHz was developed, based on the theoretical analysis described above, using GaAs Gunn diodes. The circuit was built on 5 mil Duroid 5880 material. This material was chosen for its low loss characteristics and ease of fabrication. Using the equivalent circuit configuration of Figure 2-4, the circuit layout shown in Figures 2-6 and 2-7 was fabricated. A 5 mil wide gold ribbon was connected between the Gunn diode and the microstrip circuit. The Gunn diode used was a packaged device, from Microwave Associates, with a diameter of 30 mils. The tuning varactor was a chip IMPATT device fabricated at TRW. Figures 2-8 and 2-9 show the VCO circuit and its test fixture.

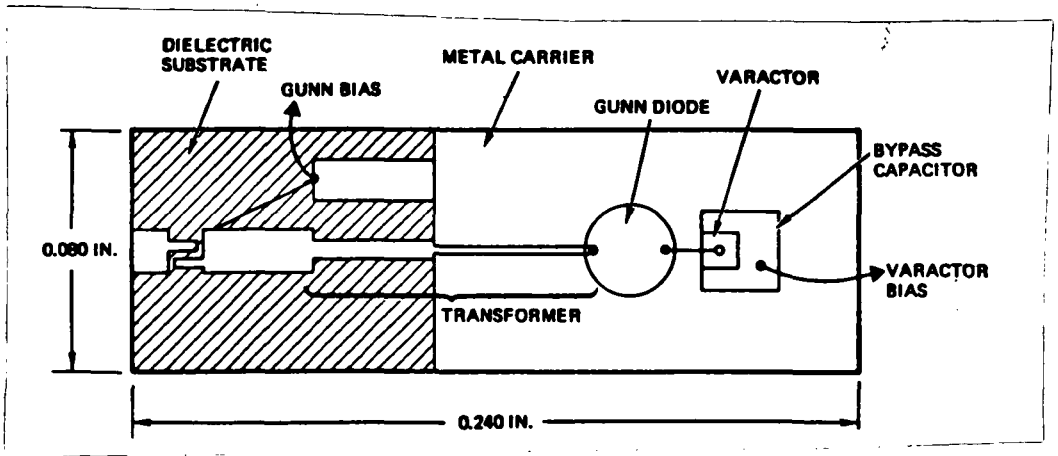


Figure 2-6. V-Band VCO (Top View)

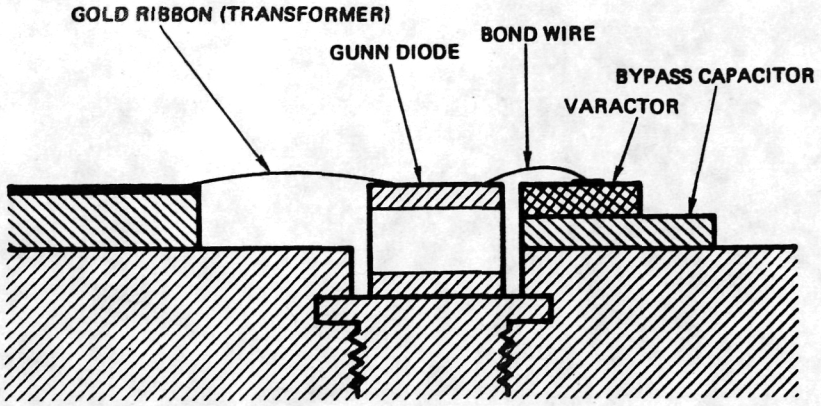


Figure 2-7. V-Band VCO (Cross-Section)

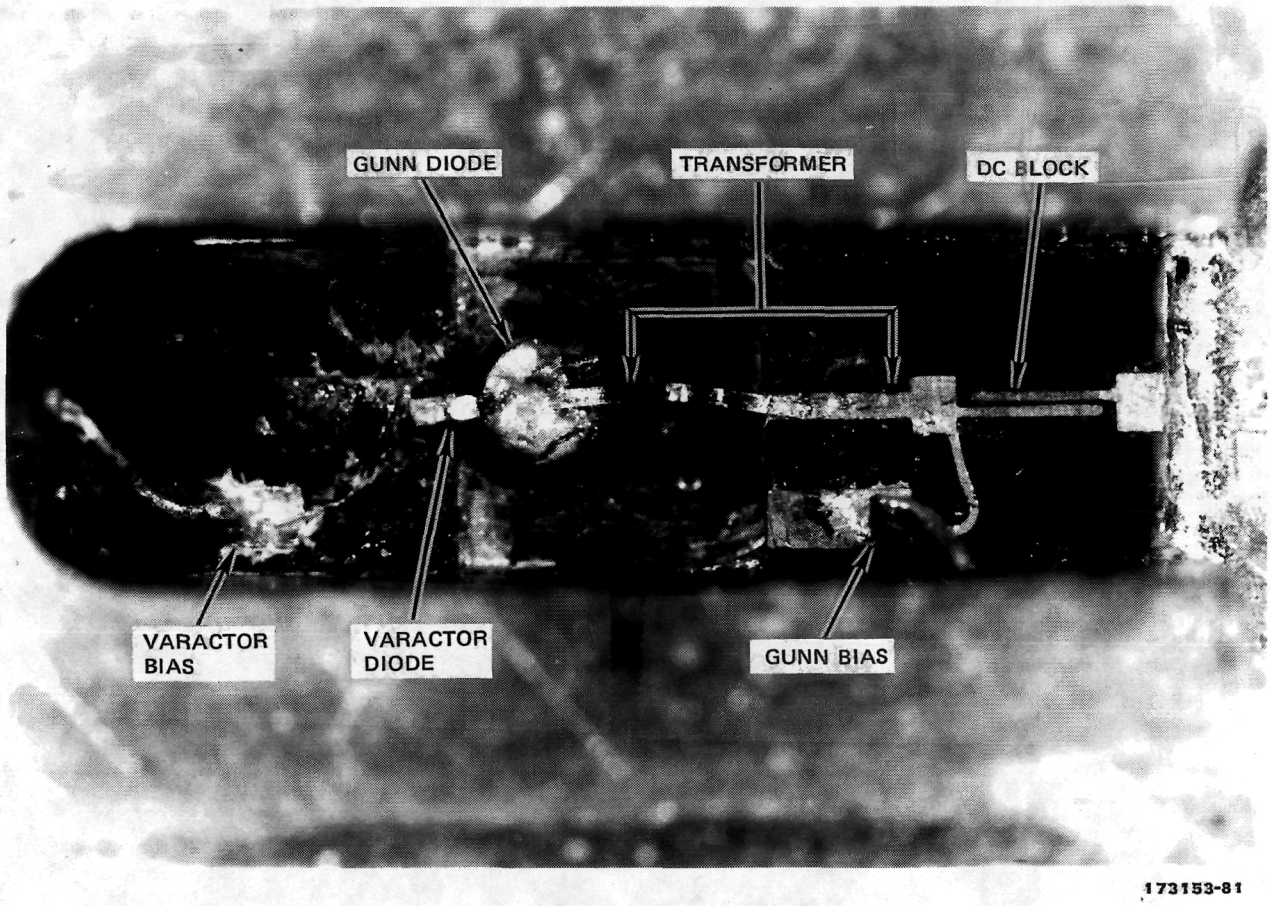


Figure 2-8. V-Band MIC Gunn Oscillator with Transition

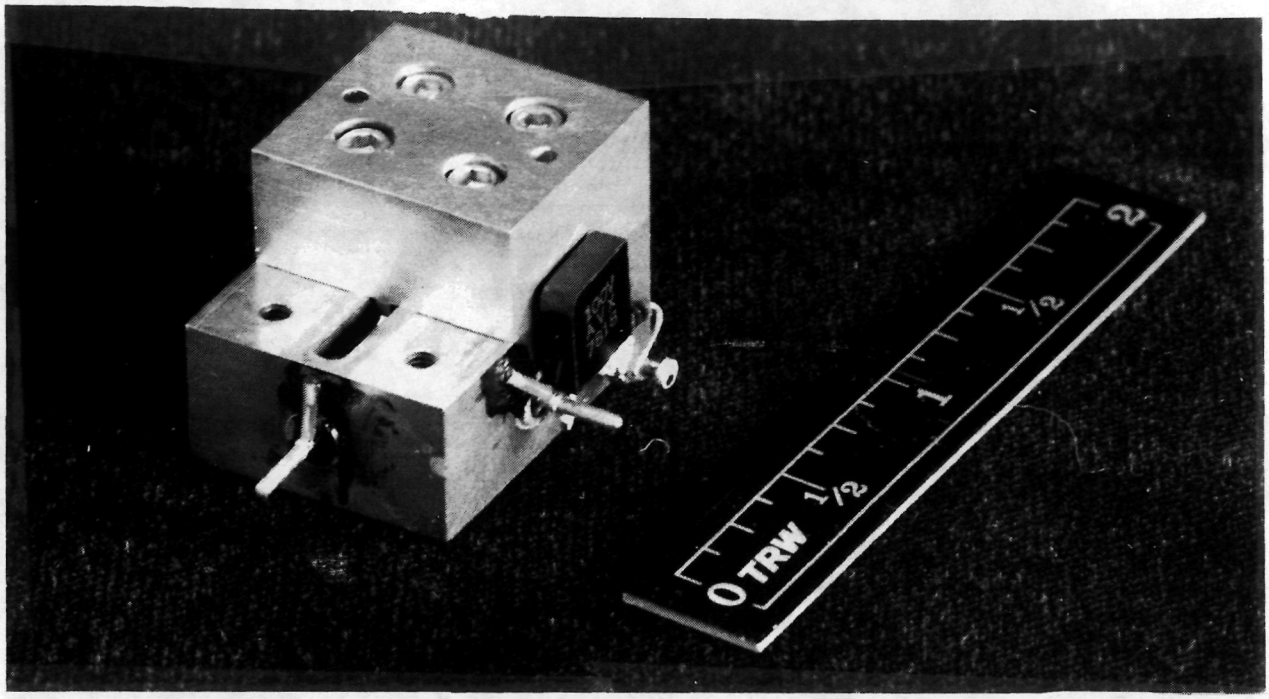


Figure 2-9. V-Band MIC Gunn Oscillator Circuit

The performance of this Gunn VCO is shown in Figure 2-10. A varactor tuning range over 500 MHz has been achieved with greater than +11 dBm output power at 60 GHz. The tuning is quite linear and the output power level is reasonably flat over the tuning range. Although a wider tuning range will help the oscillator to be locked at cold start, this tuning range is sufficient for laboratory environment. The +11 dBm output power is 1 dB higher than our proposed design goal of +10 dBm.

2.2 MIC SUBHARMONIC MIXER

A subharmonic mixer is required to mix the 60 GHz RF output from the Gunn VCO with a 14.4828 GHz reference signal to generate a 2.06896 GHz IF signal. The IF signal is then fed into the phase detector which, in turn, controls the Gunn VCO.

The subharmoinic mixer offers a simple and direct way of downconverting millimeter waves with a low frequency local oscillator. Downconversion is accomplished by mixing the millimeter wave signal with the appropriate harmonic of the LO generated in the mixer itself, thus eliminating the need for multiplier chains. The subharmonic mixers are particularly suited for phaselocked loop applications where millimeter wave sources need to be referred to a low frequency crystal controlled oscillator.

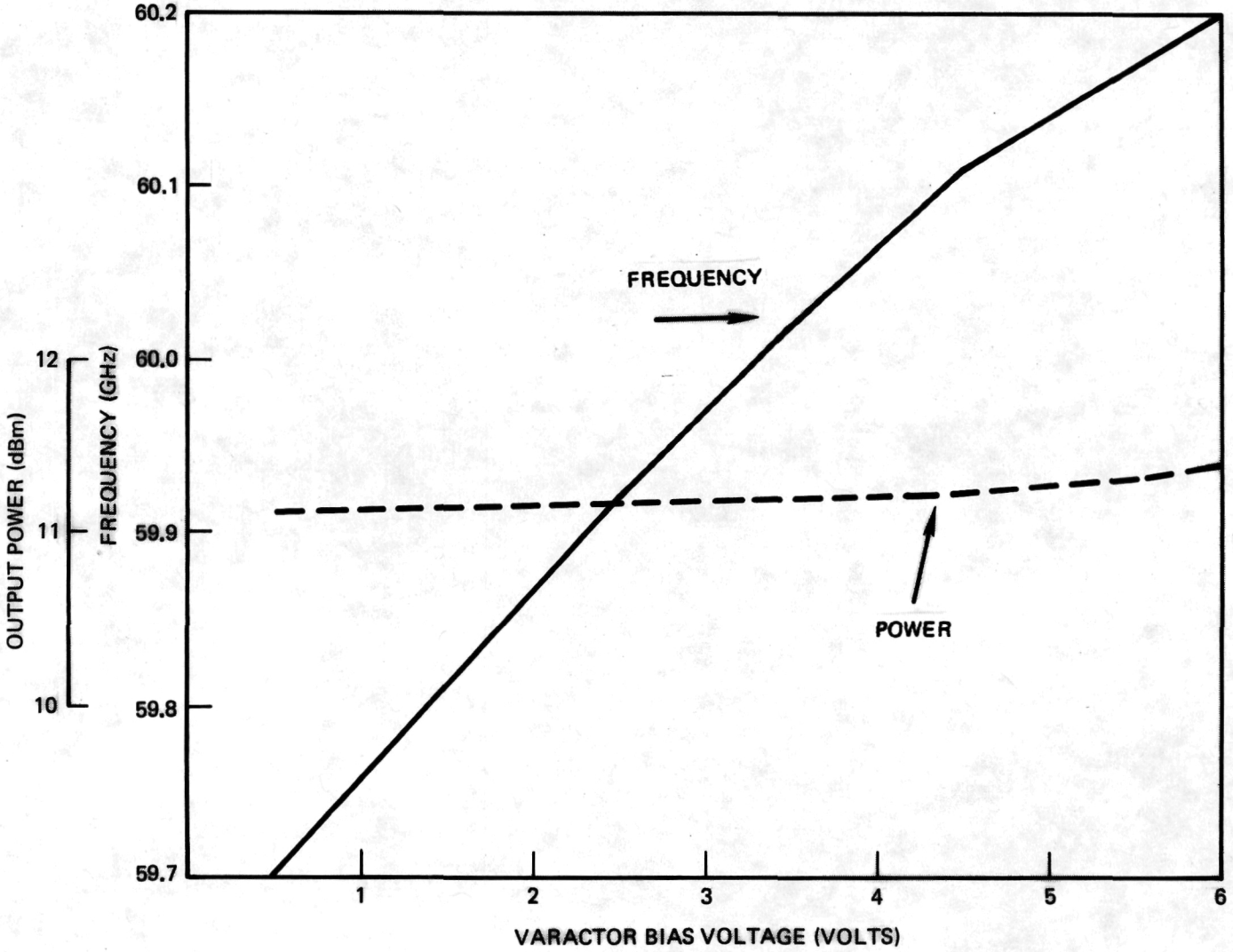


Figure 2-10. 60 GHz Gunn VCO Performance

In addition to being able to use a low LO frequency, the subharmonic mixer has the advantage of suppressing the fundamental and other odd harmonic mixing products as well as the even harmonics of the LO. The suppression of these products depends on the balance of the two diodes.

A basic schematic diagram of a subharmonic mixer is shown in Figure 2-11.

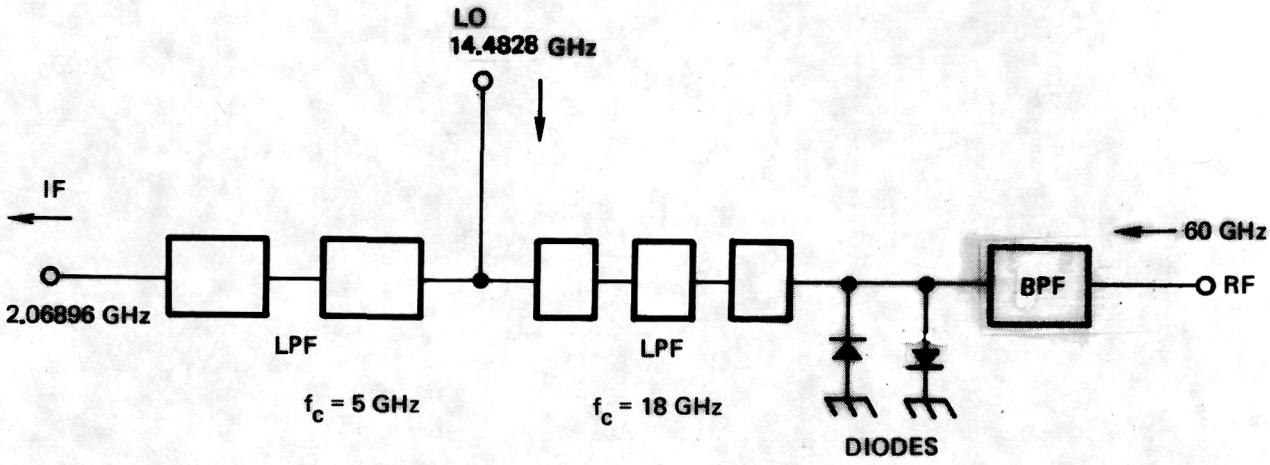


Figure 2-11. Schematic Diagram of 4th Subharmonic Mixer

In this circuit, the RF bandpass filter is used to suppress all the higher order mixing products and reject the LO and IF frequencies. A LO lowpass filter is used to transmit the LO frequency while preventing the RF from reaching the LO port. An IF filter is used as a lowpass filter to extract the IF while rejecting the LO and any residual unwanted signals from reaching the IF output port. Like the Gunn VCO, the subharmonic mixer circuit was realized using 5 mil thick Duroid 5880 material, as shown in Figure 2-12. Two beamlead diodes are used in an antiparallel configuration. To ensure proper frequency rejection, filter design is important. Figures 2-13 and 2-14 show frequency response of the LO and IF lowpass filters.

The RF bandpass filter is not critical, it is simply a quarterwave line which gives sufficient rejection at the LO and IF frequencies. Since the diodes are in an antiparallel configuration, no DC return path is needed. With minimum circuit optimization, a conversion loss of 20 dB at 60 GHz was achieved. This conversion efficiency is adequate for proper phaselocked operation.

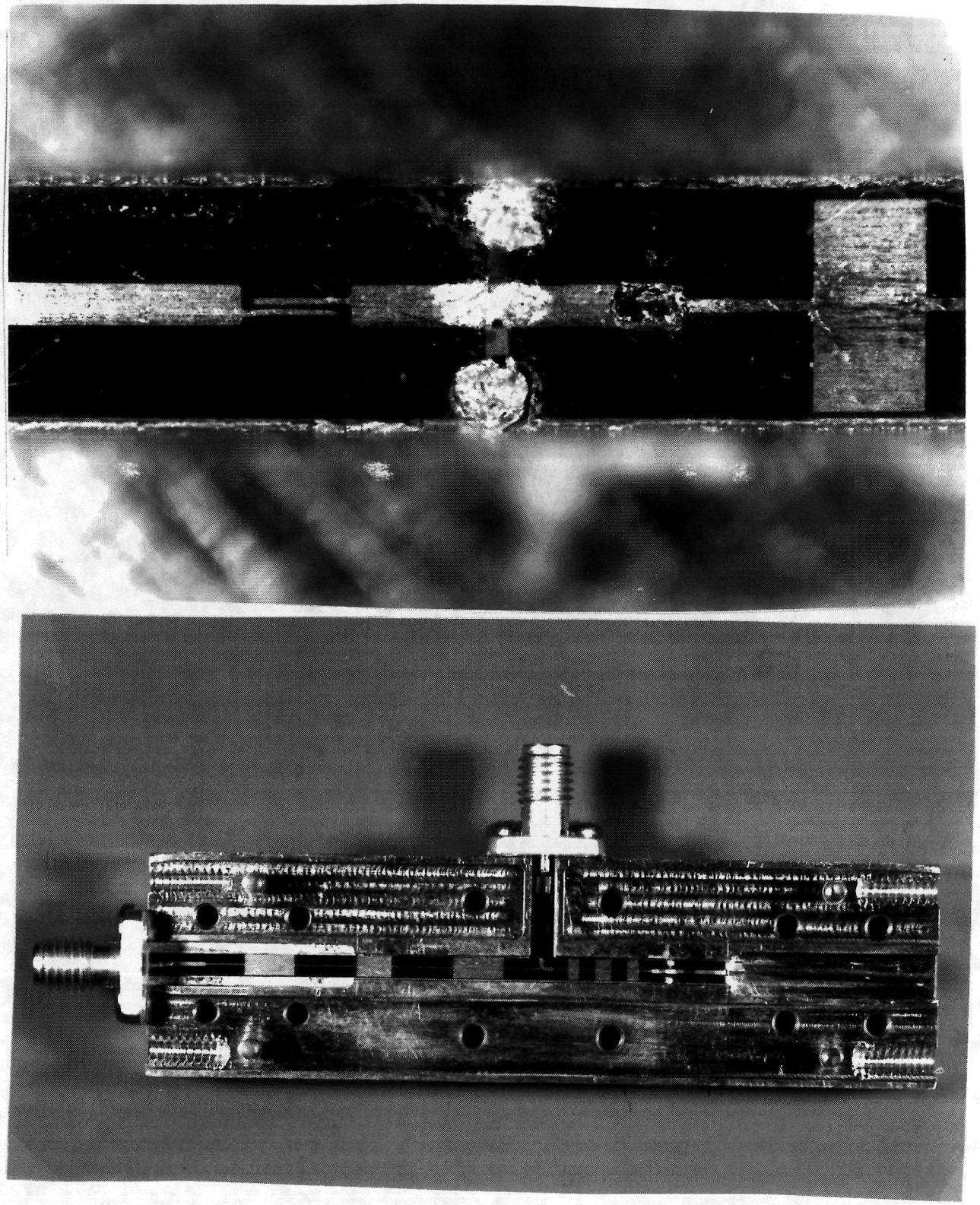


Figure 2-12. TRW V-Band 4th Subharmonic Mixer

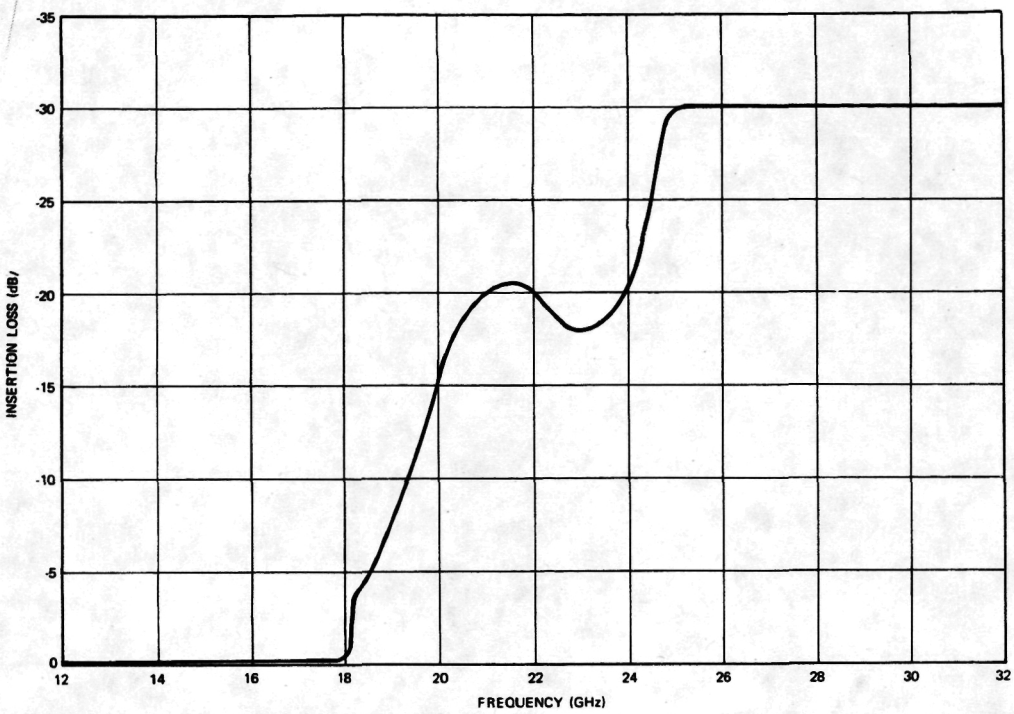


Figure 2-13. LO Lopass Filter Frequency Response

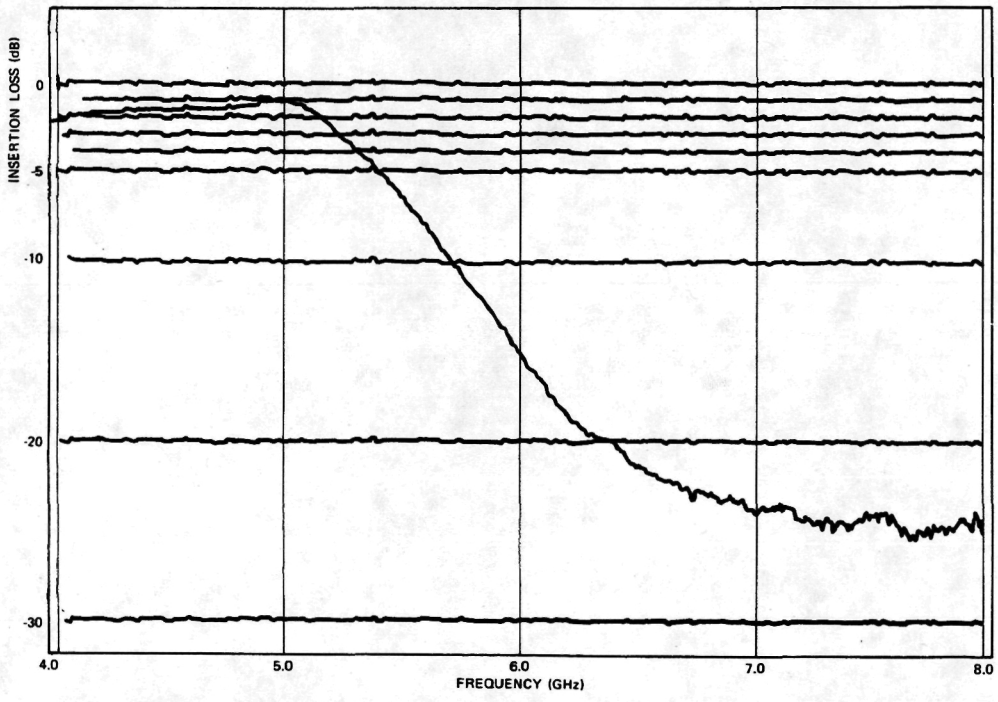


Figure 2-14. IF Lowpass Filter Frequency Response

2.3 Ku-BAND REFERENCE SOURCE

The Ku-band source consists of four major components:

- S-band reference oscillator
- S-band amplifier/reference coupler
- X7-frequency multiplier
- Power regulators provide all DC power requirements for the exciter/modulator.

A block diagram of the Ku-band source is shown in Figure 2-15, and a photograph of the source is shown in Figure 2-16.

2.3.1 S-Band Reference Oscillator

The S-band reference oscillator is a crystal-reference phaselocked source manufactured by MITEQ. It provides a stable 2.06896 GHz signal to drive the X7 multiplier and a reference output to the loop electronics used to lock the Gunn oscillator. The performance of this unit is as follows:

Frequency:	2.06896 GHz
Power Output:	+13 dBm
Spurious Rejection:	>70 dB relative to the carrier
Stability:	±30 ppm over -25 to +60°C

2.3.2 S-Band Amplifier/Reference Coupler

An HP 2N5103 transistor is used to provide 5 dB gain to increase the S-band oscillator output level to +18 dBm, which is required to drive the X7 multiplier assembly. Figure 2-17 shows the performance of the amplifier. A 15 dB directional coupler at the output supplies +3 dBm as a reference signal to the phaselock electronics.

2.3.3 X7 Frequency Multiplier/Amplifier

This unit (Figure 2-18) multiplies the S-band reference oscillator output by a factor of 7 and provides a stable 14.4828 GHz signal to drive the subharmonic mixer. The X7 is a microstrip design. The circuit consists of a driver amplifier, input isolator, and lowpass network to provide input matching and idler paths. Multiplication is accomplished with a step-recovery diode and the output frequency is selected by a three-pole comb line filter. A microstrip isolator provides isolation at the output interface. Figure 2-19 shows the circuit photomask and hardware.

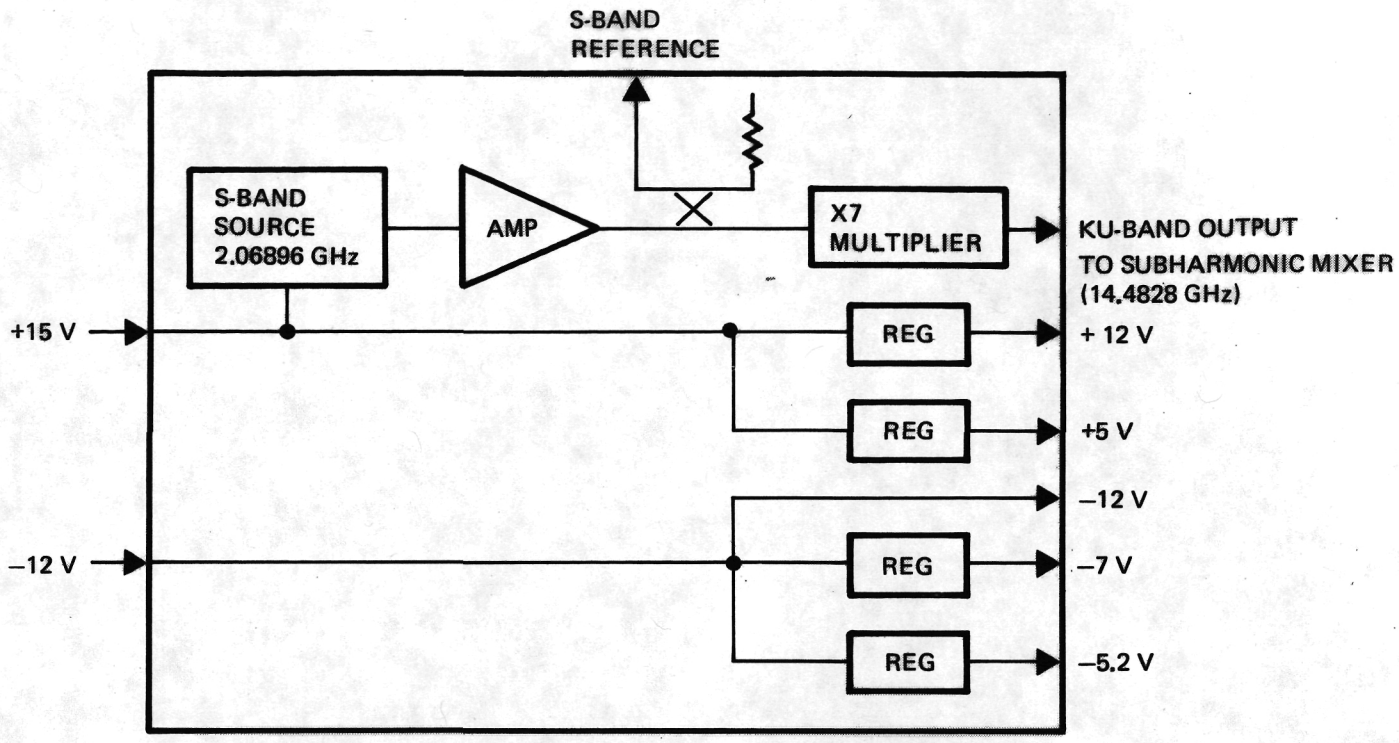


Figure 2-15. Ku-Band Source Block Diagram

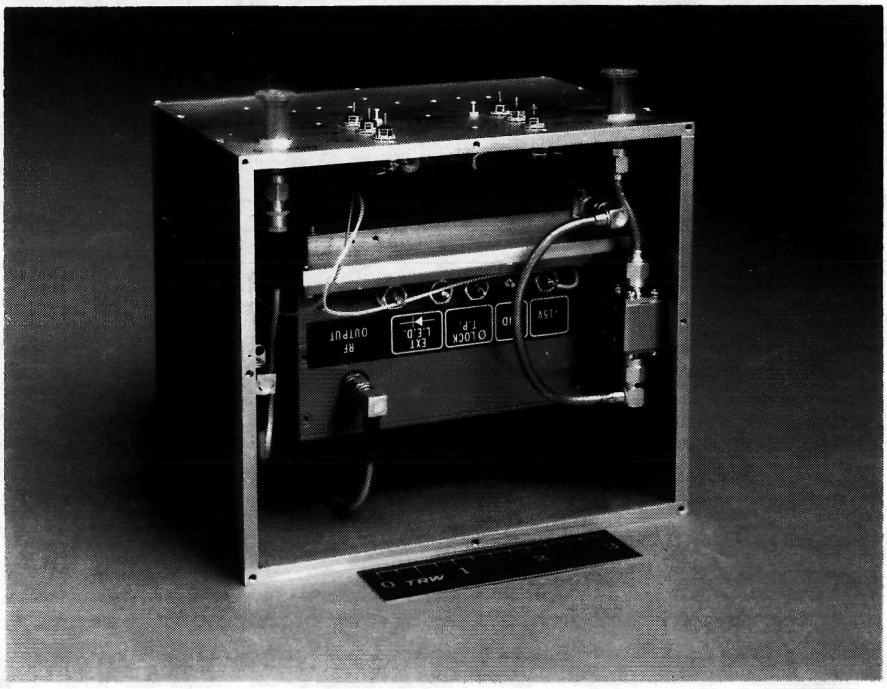
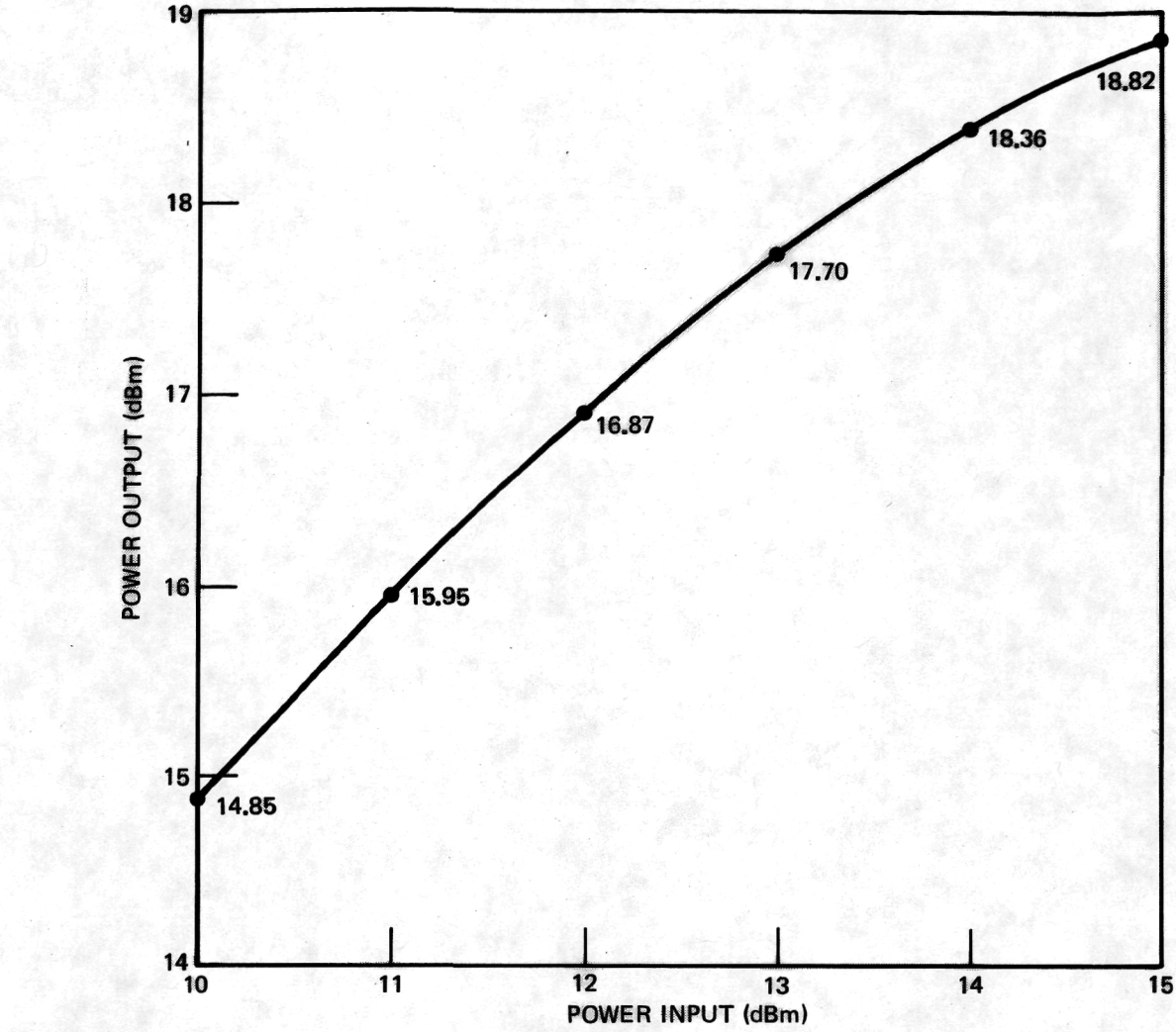


Figure 2-16. Ku-Band Reference Source Assembly



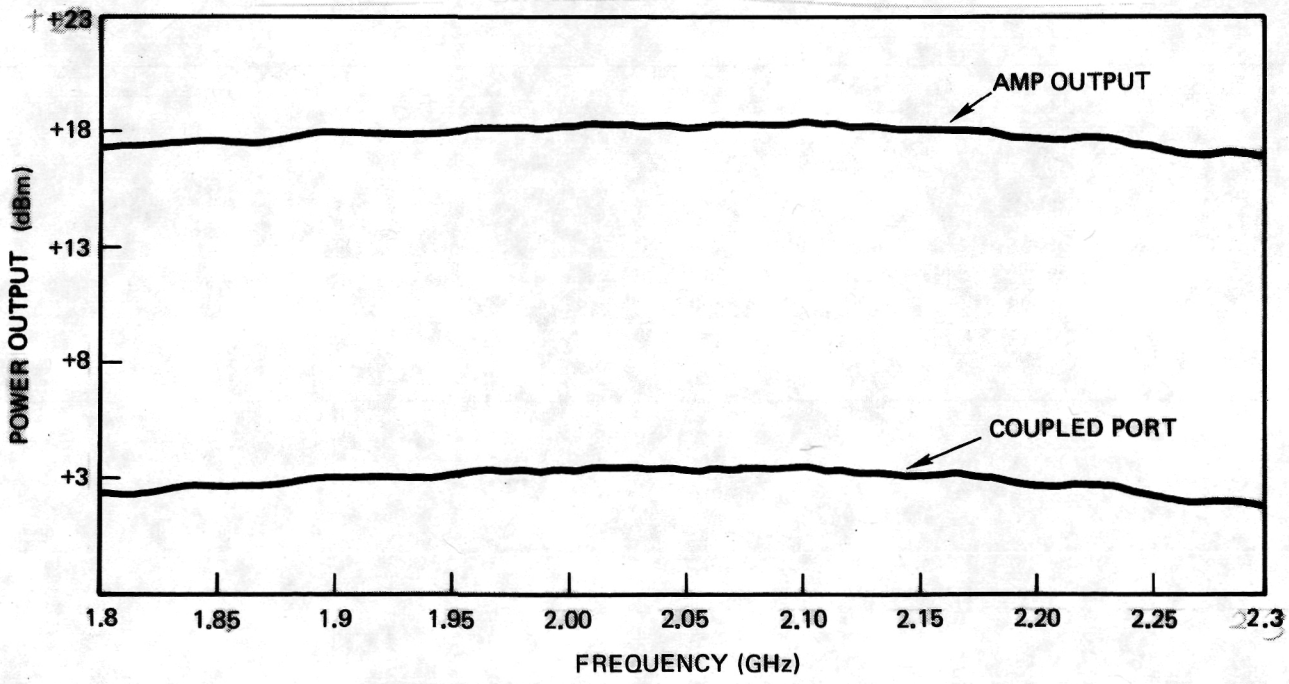


Figure 2-17. Performance of the 2 GHz Amplifier

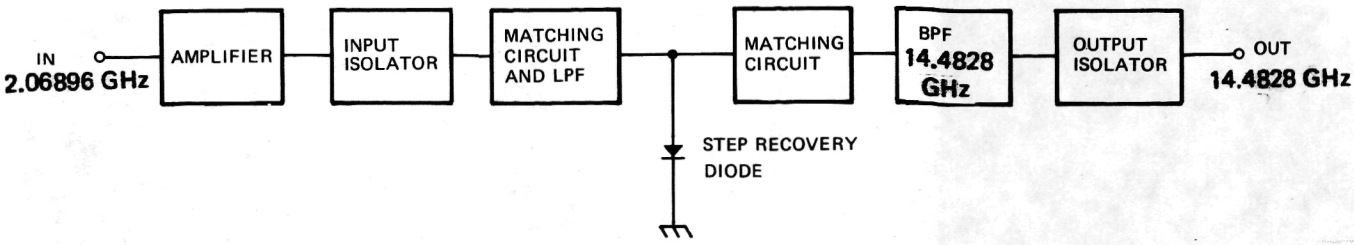


Figure 2-18. X7 Multiplier Schematic Diagram

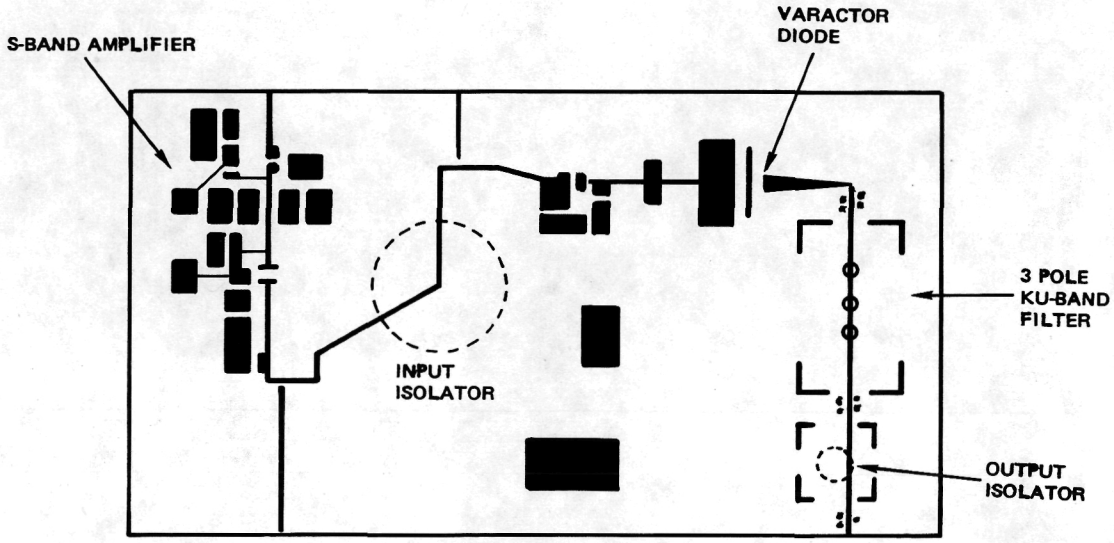


Figure 2-19. X7 Multiplier/Amplifier Circuit Photomask and Hardware

Figure 2-20 shows the equivalent circuit of the X7 multiplier. C_1, L_1 and C_2 function as a very low Q, π-network matching the input frequency into the diodes and providing a path for the idler currents to circulate for optimum efficiency. L_2 is the charging inductor and also functions as an RF block to the output frequency, preventing output signal energy from being lost in the input circuit. L_3 tunes out the reactance of the diode package at the output frequency. T_1 is a tapered matching network transforming the real impedance at the output frequency into 50 ohms at the filter input. FL1 is a 3-pole comb line filter; it selects the X7 output frequency and suppresses the drive frequency and its harmonics greater than 50 dB below the desired signal. The filter is a machined component interfacing directly with the microstrip circuitry. It features low loss (0.6 dB) for 5 percent bandwidth and small size (1.12 x 0.74 x 0.235 in.). Isolators are used at the multiplier input and output interfaces for stability under all loading conditions.

The passband frequency response of this X7 multiplier is shown in Figure 2-21. The output power as a function of input power is given in Figure 2-22.

2.3.4 Ku-Band Source Integration

The Ku-band source consists of the S-band reference source, S-band amplifier, X7 multiplier, and voltage regulators integrated into a volume of 4.2 x 5.2 x 6 in. The test results of this Ku-band source are summarized below.

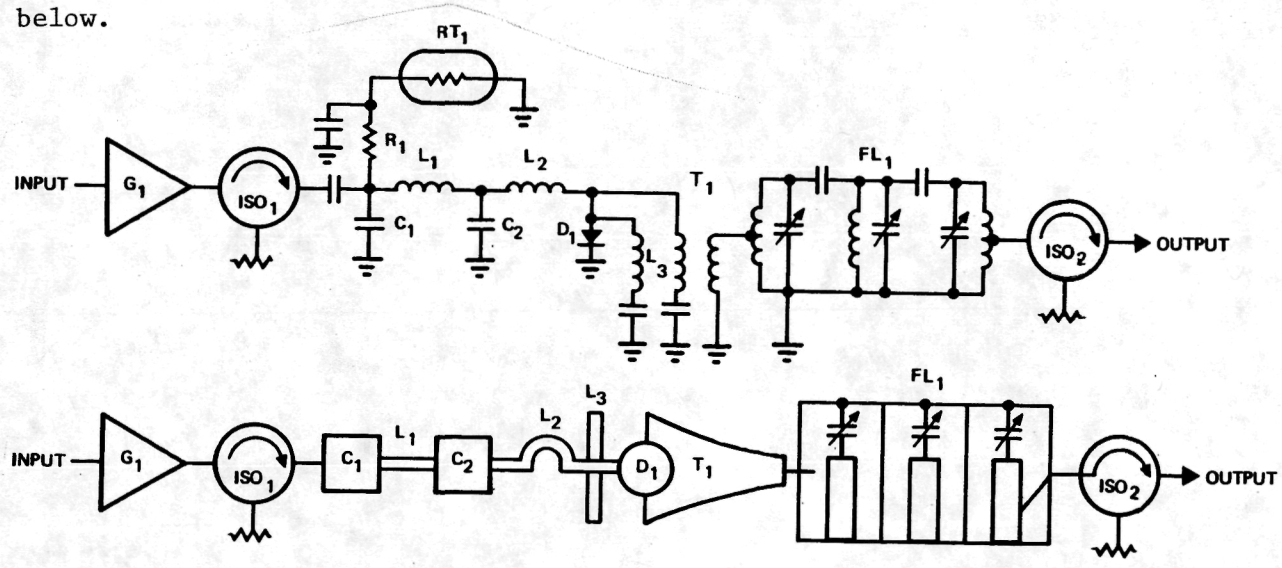


Figure 2-20. Equivalent Circuit of X7 Multiplier

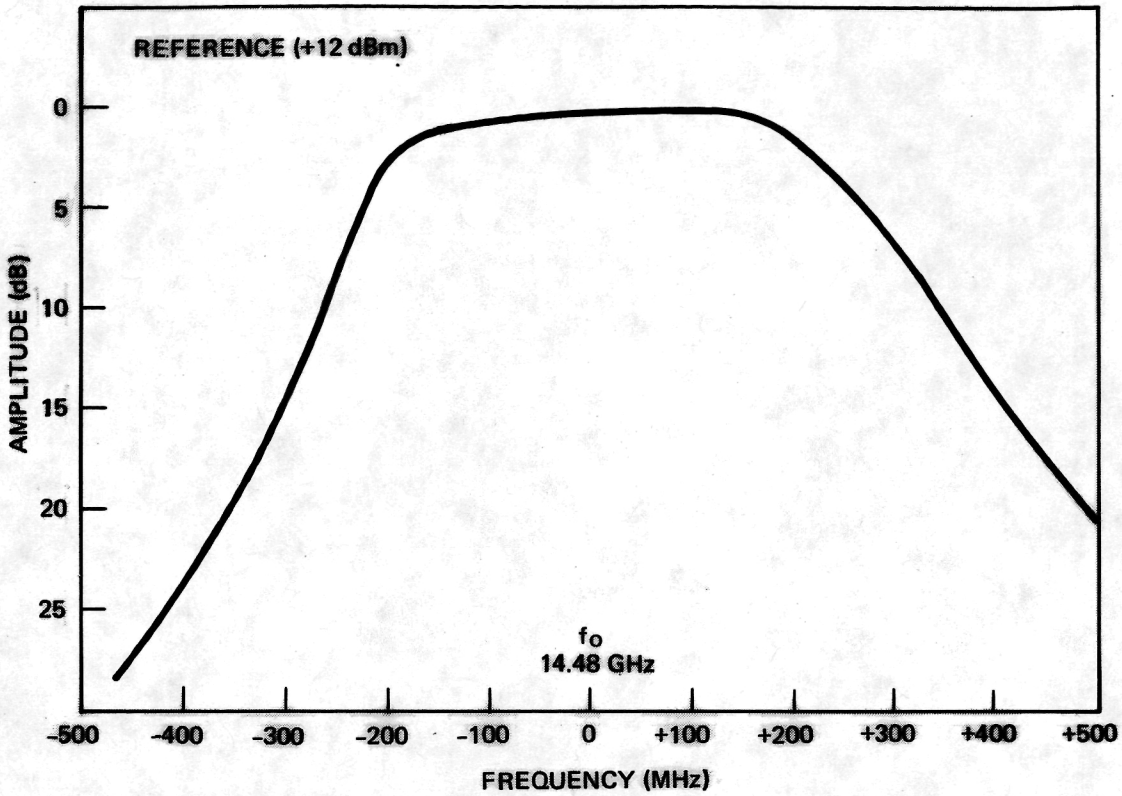


Figure 2-21. Passband Frequency Response of X7 Multiplier

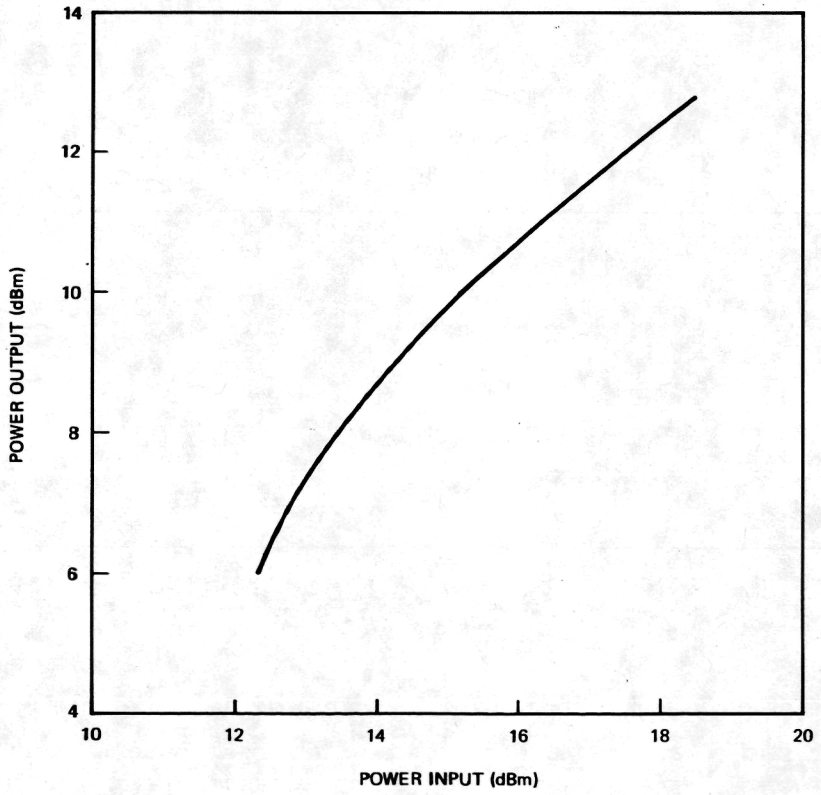


Figure 2-22. Output Power vs Input Power for X7 Multiplier/Amplifier

S-Band Output Power	+2.45 dBm
Ku-Band Output Power	+12.3 dBm
Harmonic Output	50 dB below carrier

Figure 2-23 is a photograph of the Ku-band source.

Figure 2-23. Ku-Band Source

2.4 PHASELOCK ELECTRONICS

The phaselock electronics consists of two circuit boards integrated into a volume of 4.55x4.55x1.8 in. One circuit board contains the S-band circuit and phase detectors, and the other contains the loop filter and acquisition circuits. Figure 2-24 shows a circuit diagram of these two boards.

2.4.1 S-Band Circuit and Phase Detector

The S-band circuit performs the following functions: IC7 amplifies the 2.068 GHz reference signal and splits it to provide an in-phase LO signal to the sine and cosine phase detectors. An attenuator of 7 dB at the input is used to establish the proper LO/RF ratio at the mixer. IC1, IC2, IC5 and IC6 amplify the downconverted subharmonic mixer output signal and split this signal in a 90° hybrid to drive the sine and cosine phase detectors. The phase detectors compare the downconverted RF signal with that of the crystal reference source to produce two output signals (sine and cosine).

Since the subharmonic mixer input power may vary, an AGC loop is incorporated. IC3, PS2, IC4 and IC8 make up an AGC loop which, in turn, will maintain the sine and cosine phase detector input levels within ±0.3 dB for subharmonic mixer output variations of ±5 dB.

The heart of the phase detector electronics is two S-band balanced mixers from Watkins Johnson (WJ M4G). The IF outputs provide the sine and cosine waveforms from the subharmonic mixer 0° and 90° outputs, respectively. Sensitivities are 120 mV peak-to-peak for sine detector and 160 mV for cosine detector.

Figure 2-25 is a photograph of the circuit layout. The reference channel provides 12 dB of gain from the reference input to the phase detector LO inputs.

The signal channel open loop gain (no AGC) is in excess of 30 dB for the 0° and 90° outputs. With the AGC circuit enabled, signal channel gain is maintained at 20 dB. The results are shown in Figures 2-26 and 2-27.

2.4.2 Loop Filter/Acquisition Circuits

The purpose of the loop filter/integrator (U1) is to maintain phase-lock with the desired loop bandwidth and damping. The phase error signal is converted to a DC voltage that controls the varactor tuning of the Gunn

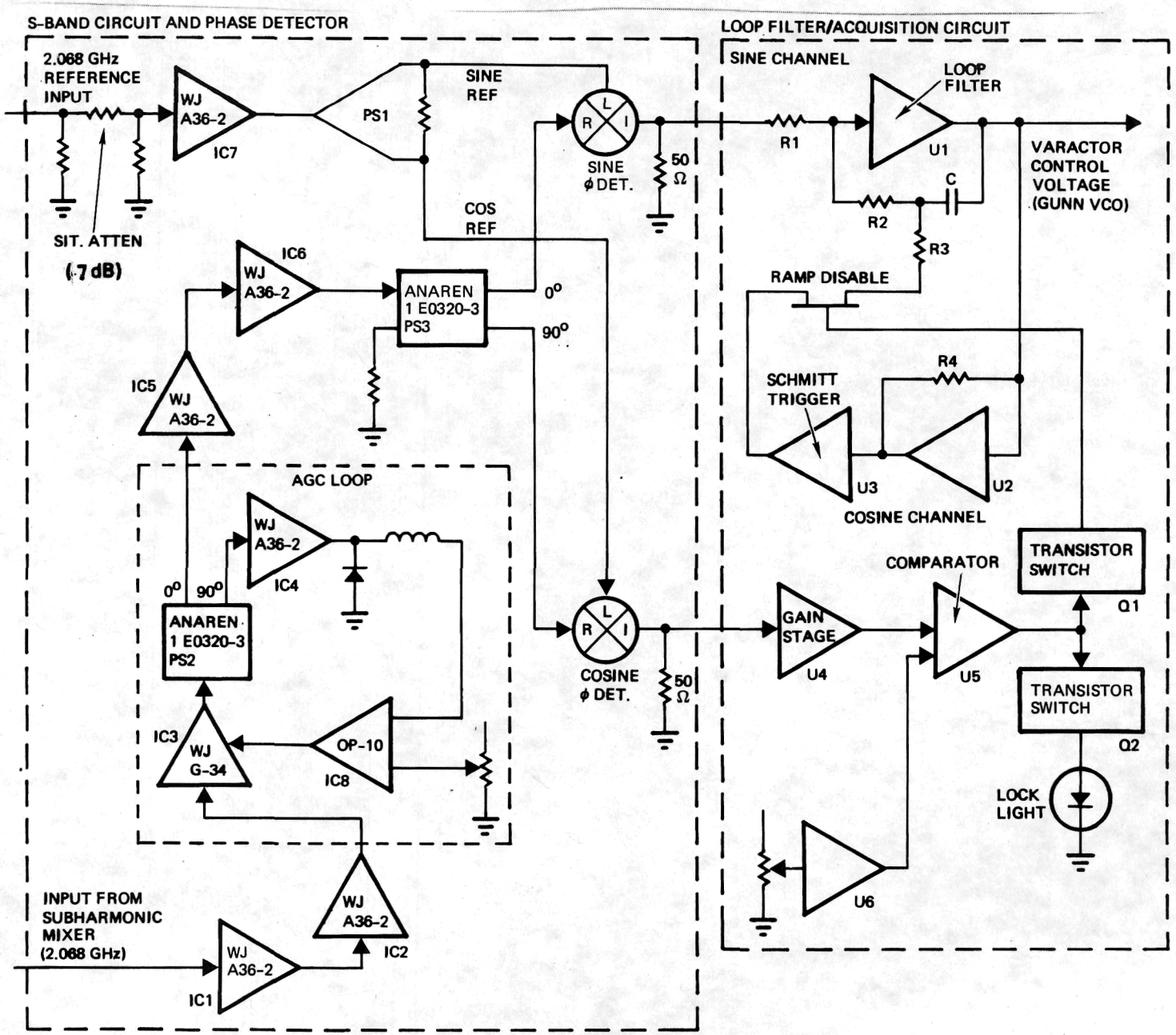


Figure 2-24. Circuit Diagram of Phaselock Electronics

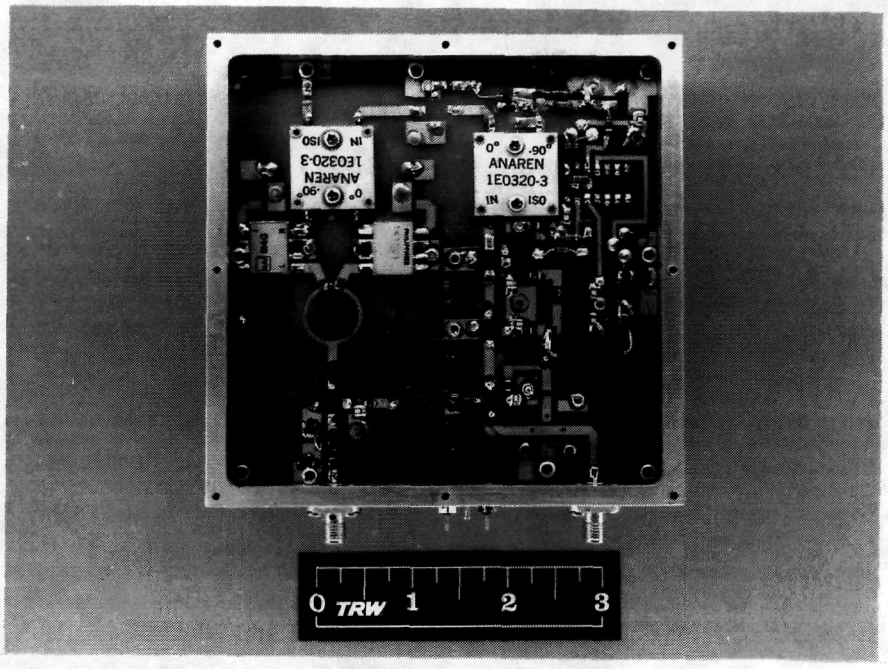


Figure 2-25. Phaselock Loop and Phase Detector Assembly

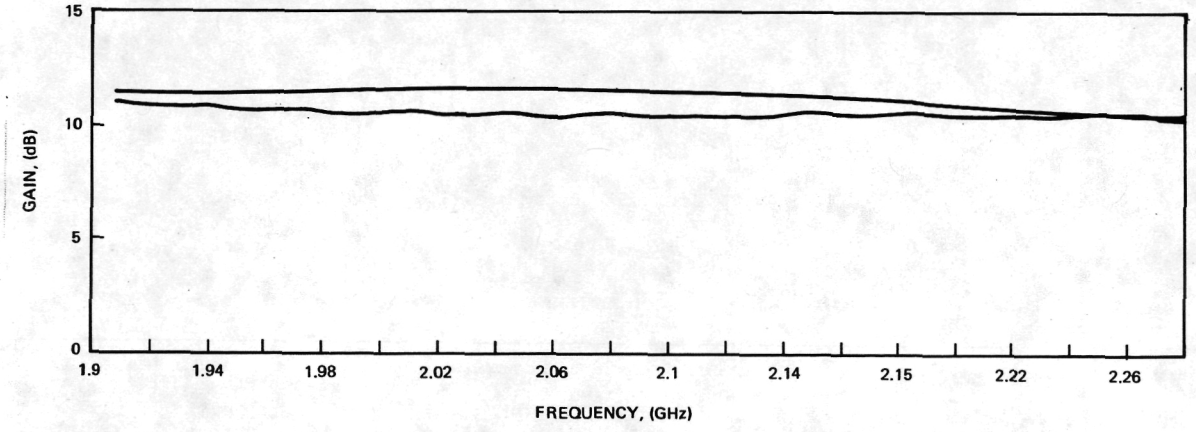


Figure 2-26. Reference Channel Gain

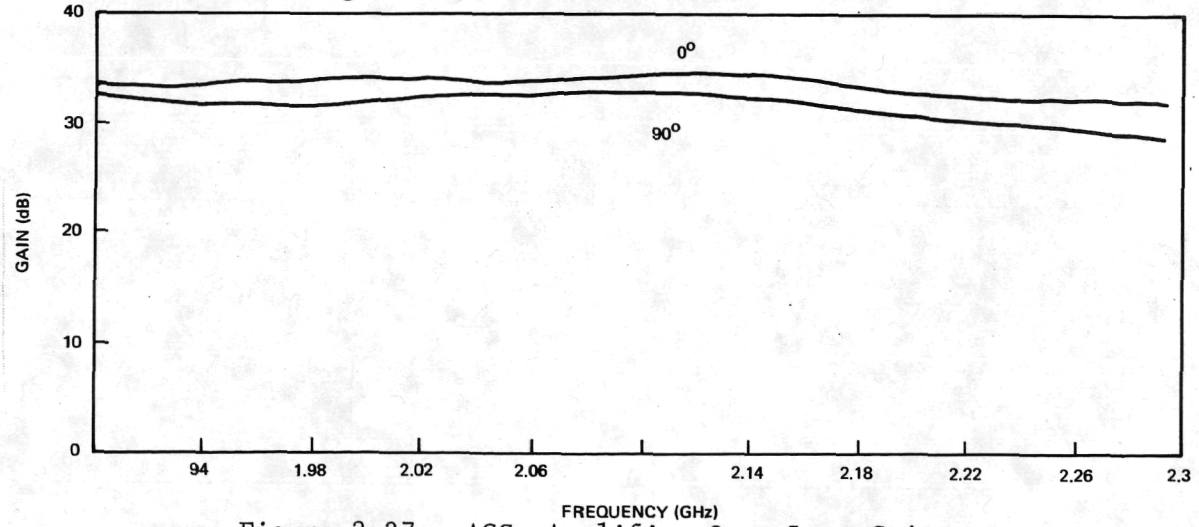


Figure 2-27. AGC--Amplifier Open Loop Gain

oscillator, thus providing the desired frequency correction. At initial turn-on, or at temperature extremes, the Gunn VCO frequency may be well out of the loop capture range. Therefore, some means must be provided to assist the loop in acquiring lock. The acquisition circuits consist of an analog loop filter and a ramp search circuit. The ramp search circuit is used during cold start to acquire the signal. Upon acquisition, the ramp search circuit is essentially disabled and the Gunn VCO is steered by the analog loop filter. The advantages of this ramp search circuit compared to previously used digital loop circuits are its simplicity and lower noise.

Two outputs, sin $\emptyset$ and cos $\emptyset$ from the phase detector, are fed into the frequency acquisition circuits shown in Figure 2-24. The output of the loop filter controls the varactor tuning of the Gunn oscillator and can be adjusted to set the Gunn VCO operating frequency.

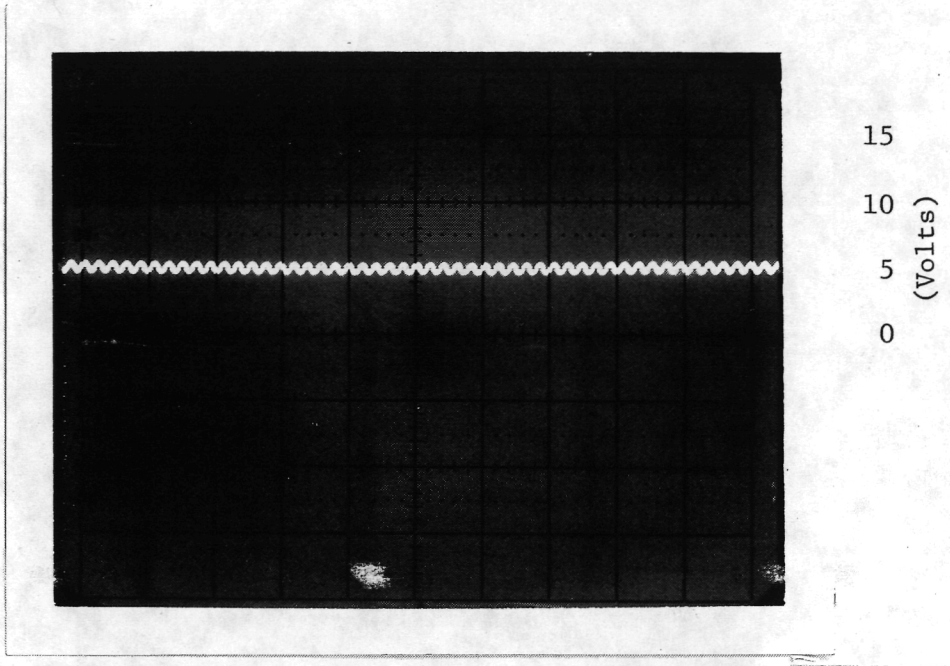
Figure 2-28 shows the loop filter output signal with ramp disabled and open loop conditions. Figure 2-29 shows loop filter output with the aided acquisition (ramp search) activated. Once the Gunn VCO is locked, the ramp sweep is disabled and a lock light is turned on.

2.5 EXCITER PERFORMANCE SUMMARY

The performance of our QPSK exciter is summarized below.

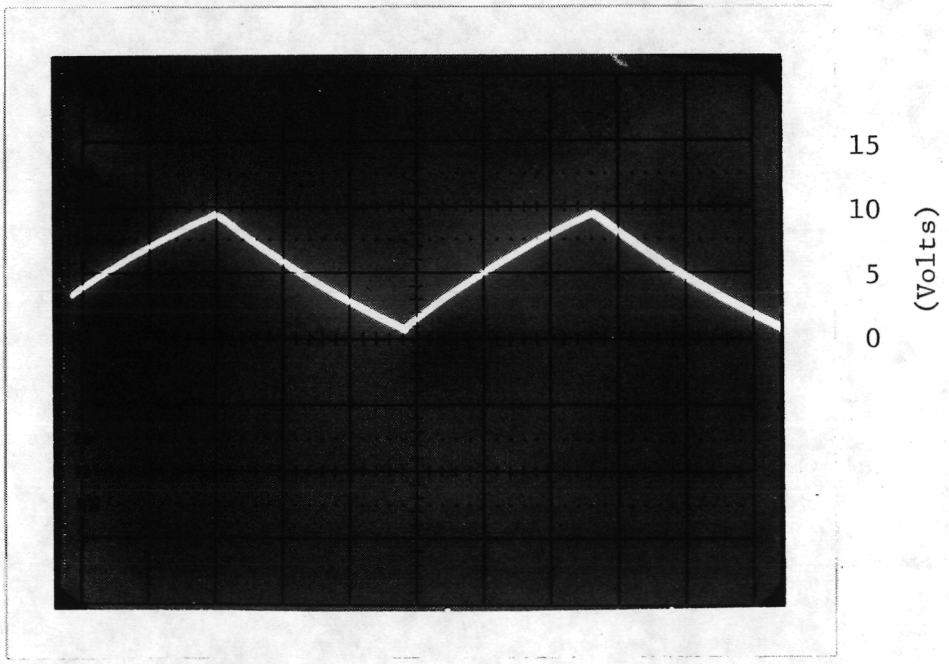
Power Output	+11 dBm
Capture Range	±10 MHz
Lock Range	-180 MHz to +160 MHz
Loop Bandwidth	2 MHz

Figure 2-30 shows the spectrum of a free running Gunn oscillator and the phaselocked output spectrum. It can be seen that a very clean signal has resulted from the phaselock. The inner noise pedestal is due to the multiplied phase noise and loop bandwidth of the S-band source.



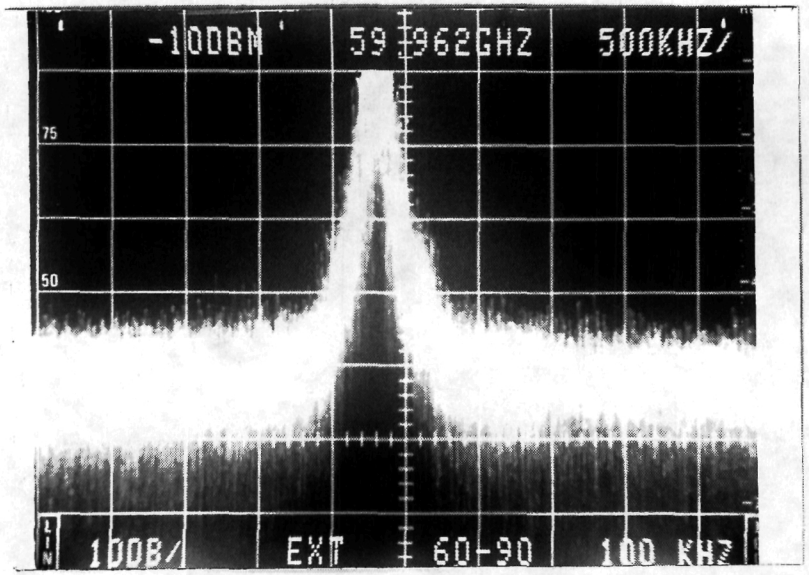
5 ms/div.

Figure 2-28. Output of Loop Filter with the Ramp Circuit Disabled and Open Loop

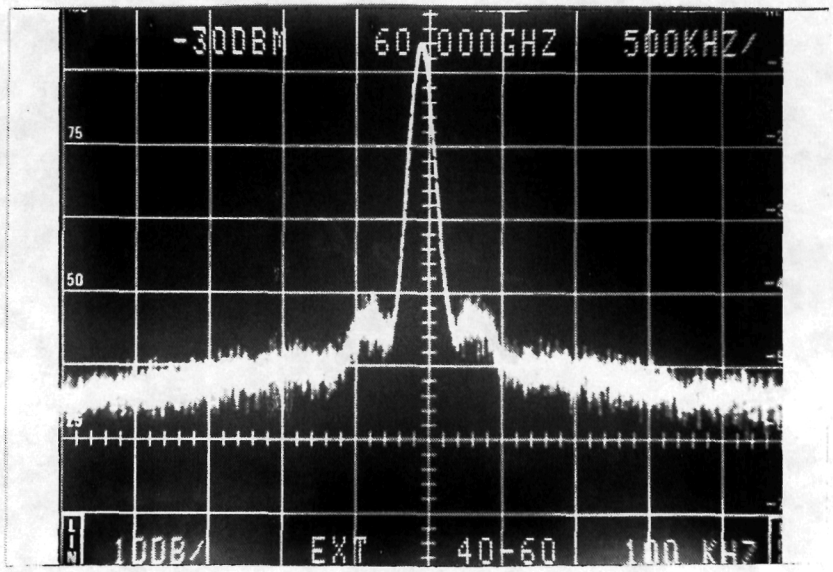


10 μs/div.

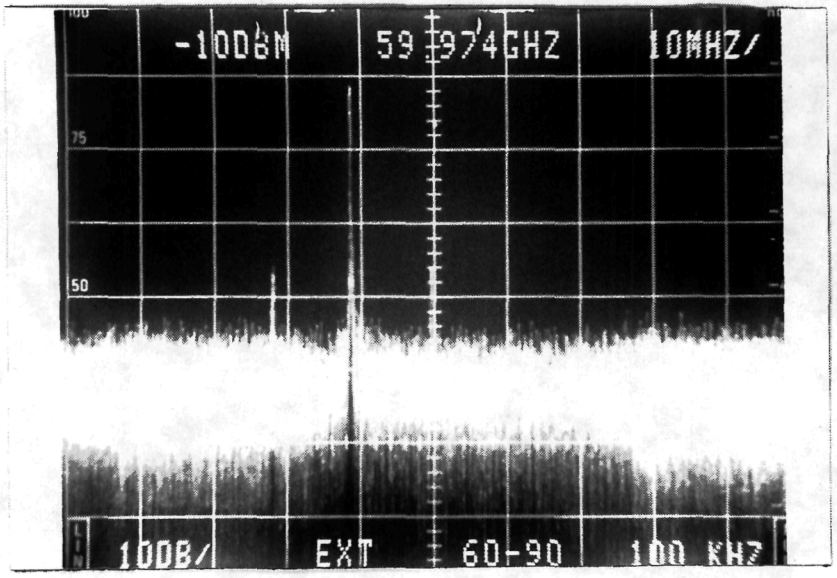
Figure 2-29. Output of Ramp Circuit with Loop Filter Disabled



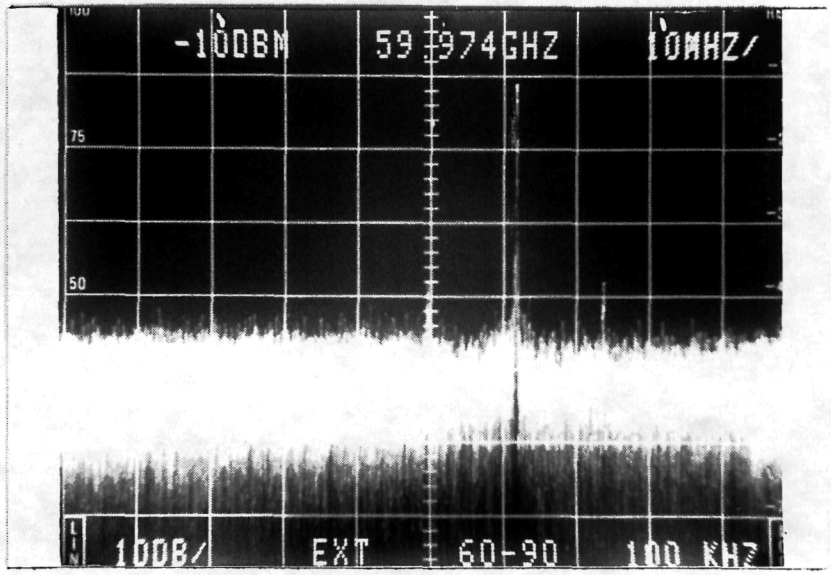
(a) Spectrum of a Free-Running Gunn Oscillator.
Horizontal Scale: 500 kHz/div.



(b) Spectrum of a Phase-Locked Gunn Oscillator.
Horizontal Scale: 500 kHz/div.



(c) Capture Range Measurement.
Horizontal Scale: 10 MHz/div.



(d) Capture Range Measurement .
Horizontal Scale: 10 MHz/div.

Figure 2-30. Spectrum of Gunn VCO

3. QPSK MODULATOR DEVELOPMENT

A block diagram of the QPSK modulator is shown in Figure 3-1. The circuit consists of a Wilkinson power splitter with a 90° phase shift introduced in one leg, two biphase switches, an in-phase power combiner, and a microstrip-to-waveguide transition at the output. This configuration offers a simple and direct approach to generating a QPSK modulated signal.

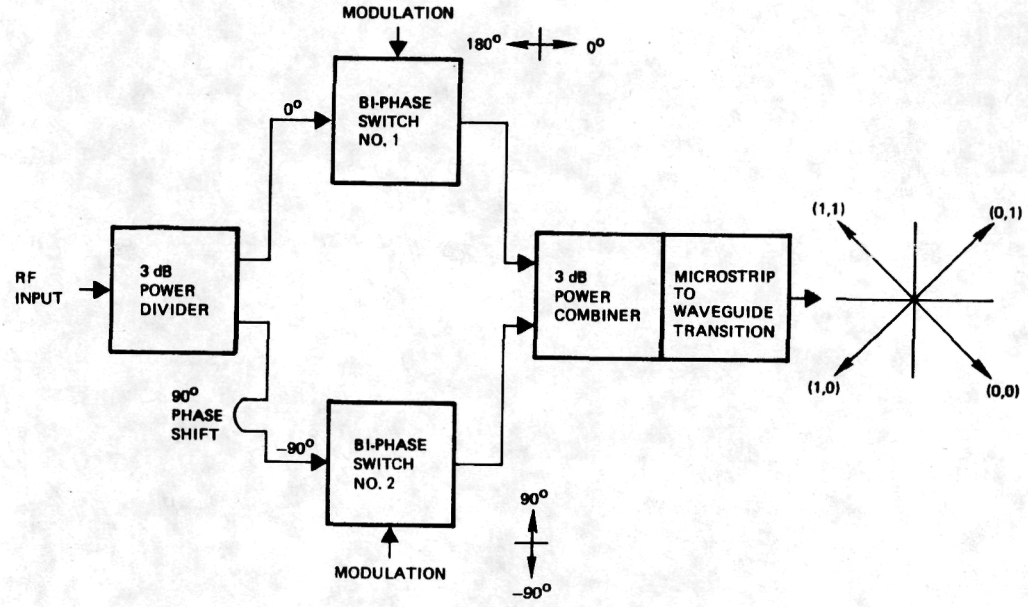


Figure 3-1. QPSK Modulator Block Diagram

Figure 3-2 shows the QPSK circuit layout [2]. In this figure, the dotted lines indicate microstrip on the reverse side of the substrate, while the solid lines indicate slotlines on the substrate. The only exception to this is the data filters. The data filters are microstrip, represented by solid lines on the substrate, while the microstrip ground plane is represented by dashed lines on the reverse side of the board. A photograph of this chip fabricated on sapphire substrate is shown in Figure 3-3.

The circuit operates as follows: The unmodulated RF carrier enters the circuit on microstrip and goes to the in-phase power divider. The signal is divided into two equal amplitude in-phase signals. One arm of the power divider drives the biphase switch #1 directly. A 90° phase shifter is introduced at the input of biphase switch #2. This is achieved by increasing the microstrip path length between the power divider and biphase switch #2.

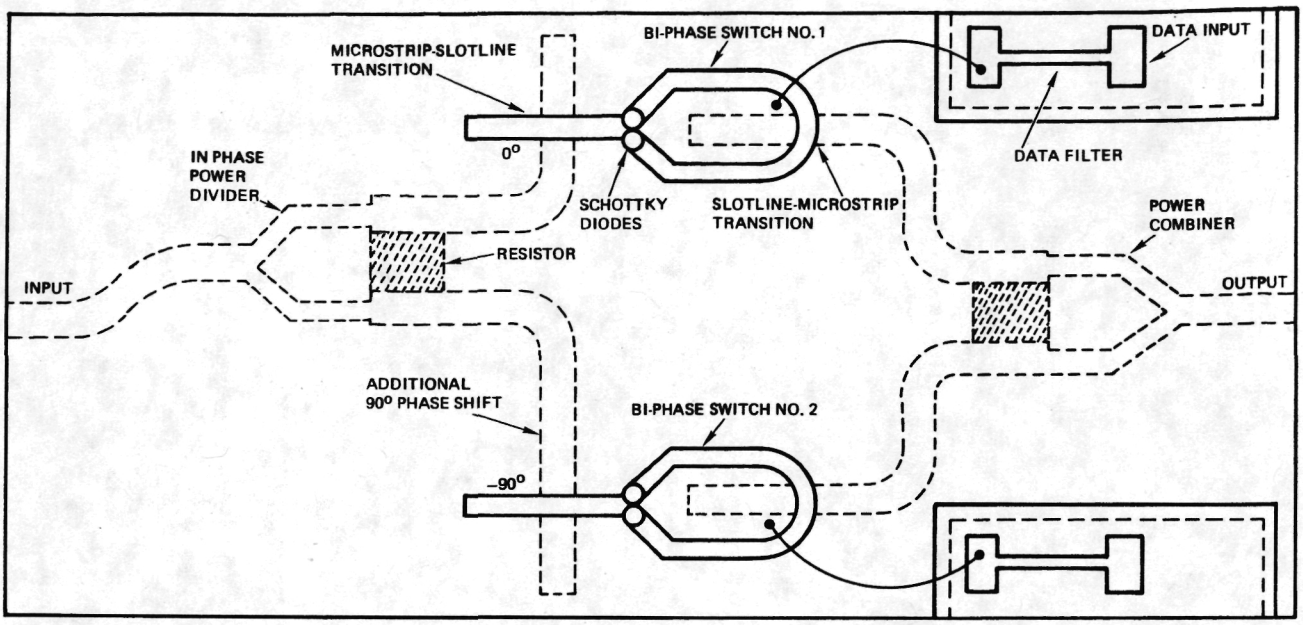


Figure 3-2. QPSK Circuit Layout

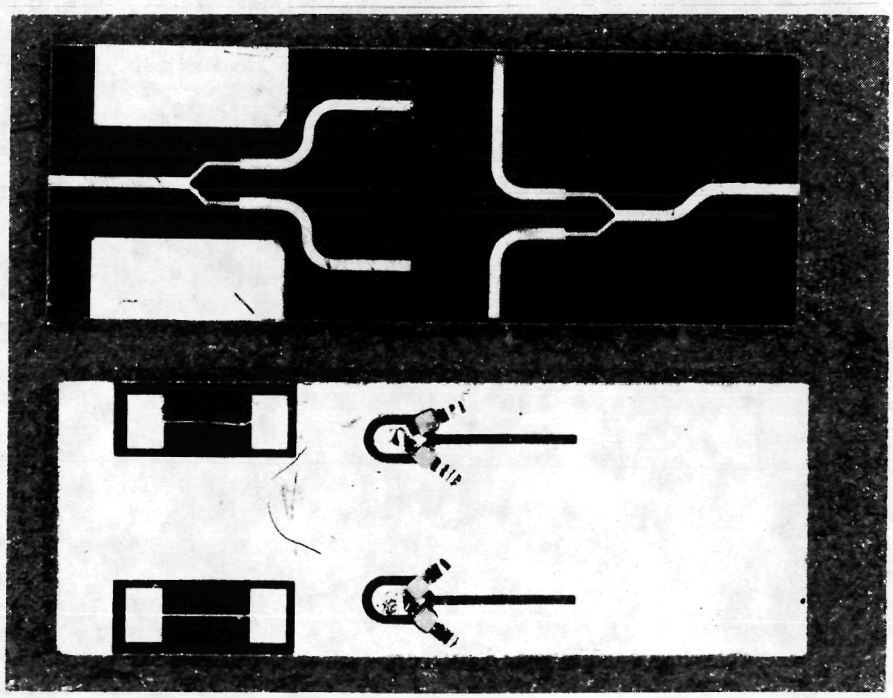


Figure 3-3. QPSK Modulator (Shown are both sides of the chip.)

The biphase switches introduce an additional 0° or 180° phase shift to each signal as the data inputs switch the Schottky diodes. The two biphase modulated signals are then summed in an in-phase power combiner producing a quadriphase modulated signal.

The modulator used has the following advantages:

1. High isolation between the carrier input port and the modulated carrier output port is obtained due to the balanced configuration.
2. Instead of using a 90° hybrid, the 90° phase shift is introduced by path length. This simplifies the design since a low loss, well-balanced 90° hybrid is difficult to realize at 60 GHz.
3. A DC return path is not required because slotlines are used.
4. The 180° phase shift is introduced by the built-in field distribution of the slotline.
5. A simple configuration using only a wire bonding is sufficient for baseband input circuit.
6. Small size is achieved by using sapphire substrate.

3.1 POWER DIVIDER/COMBINER

Two designs were considered for the 90° power divider: a 90° branch line coupler and an in-phase divider with a 90° length of transmission line in one leg. The 90° branch line is a more complicated structure and requires compensation at the junctions that are difficult to fabricate at 60 GHz. As an example, a 35-ohm line is required in the branch-line coupler. With a 5-mil thick sapphire substrate, a line width of 9 mils is required. This line has a quarter wavelength of 18 mils at 60 GHz. Thus a quarter wavelength is only twice as long as its width and junction effects dominate the circuit response. The in-phase divider was chosen based on its less complicated structure.

The three-port Wilkinson type hybrid was selected for its simplicity and good performance [3]. As shown in Figure 3-4, power entering the shunt port emerges with equal amplitude and phase at the other two ports. Each of the three ports has nearly unity VSWR, while isolation of the output port is high.

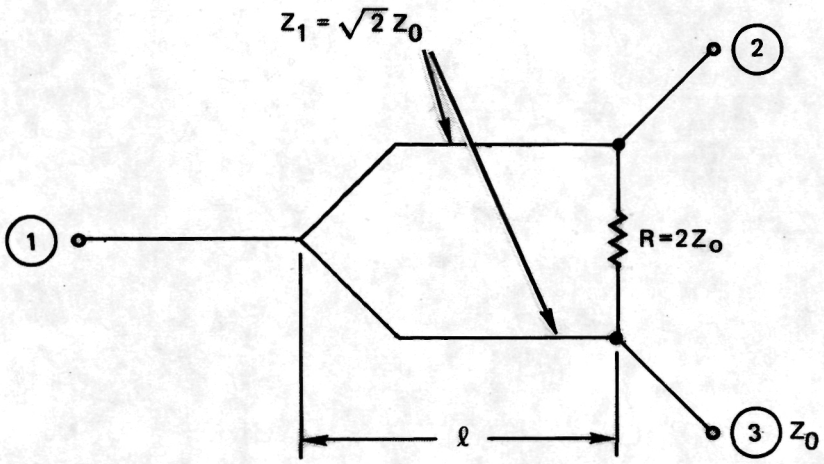


Figure 3-4. Wilkinson's 3 dB In-Phase Power Combiner/Divider

In addition to its application as a power divider, reciprocity allows this type of hybrid junction to function as a low loss combiner.

Initial design and characterization was done at 15 GHz using Duroid 6010 substrate, which has a dielectric constant of 10.5 similar to that of sapphire. Figure 3-5 shows the performance of the 15 GHz hybrid on Duroid 6010 substrate. It can be seen that the amplitude balance at 15 GHz is excellent. The insertion loss of the hybrid is less than 1 dB and the isolation of the two output ports is over 20 dB. The resulting design was scaled to 60 GHz using sapphire substrate.

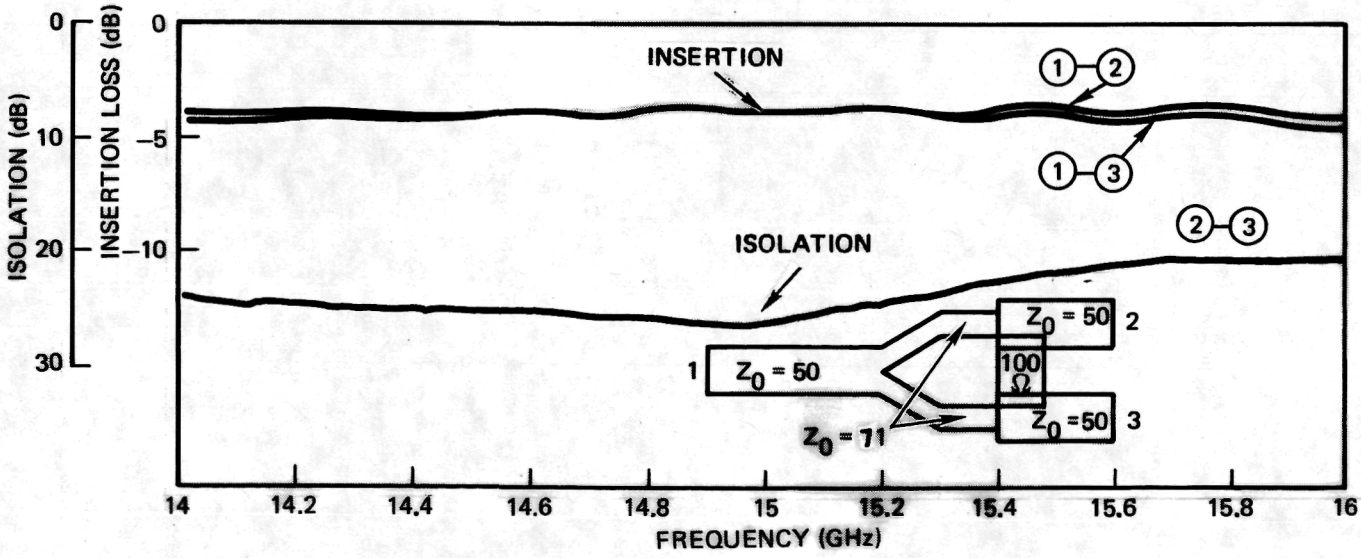


Figure 3-5. Performance of 15 GHz Hybrid on Duroid 6010 Substrate

3.2 60 GHz SLOTLINE BIPHASE SWITCH

The biphase switch is the key component in the QPSK modulator. Figure 3-6 shows the circuit configuration of the biphase switch. The circuit consists of two microstrip-to-slotline transitions, two beamlead Schottky-barrier diodes, two λ/4 slotline paths, and a microstrip low pass filter.

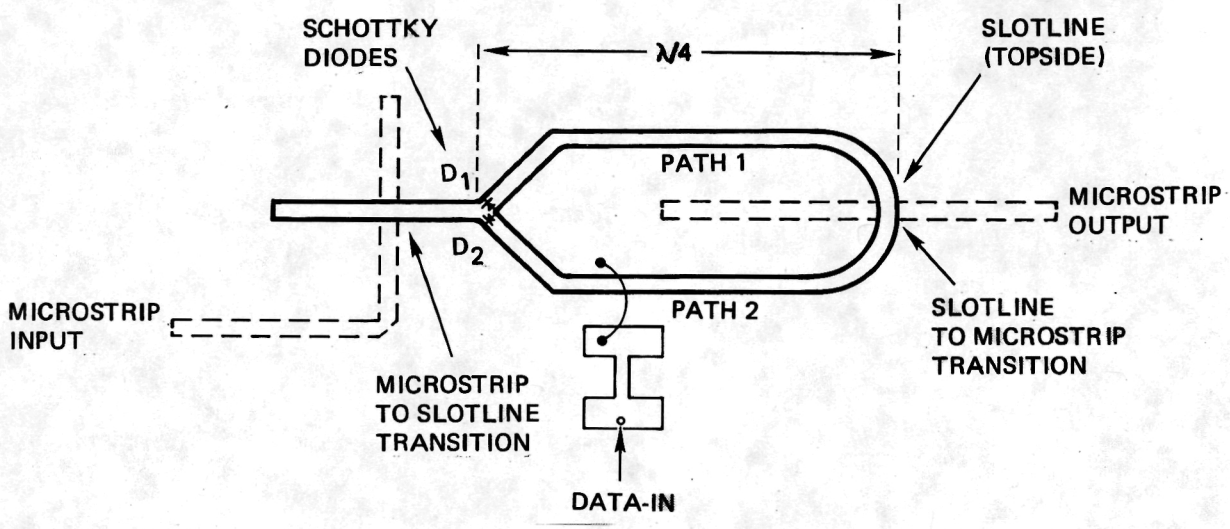


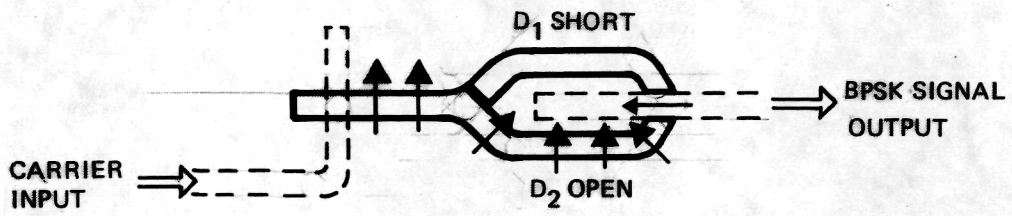
Figure 3-6. Schematic of a Biphase Switch

The design utilizes a minimum of components to accomplish biphase modulation with low loss and wide bandwidth.

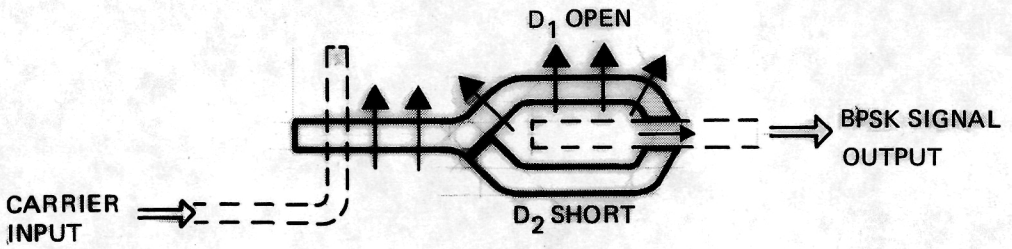
The balanced configuration provides good isolation between the input carrier and the modulated output port.

3.2.1 Operating Principle

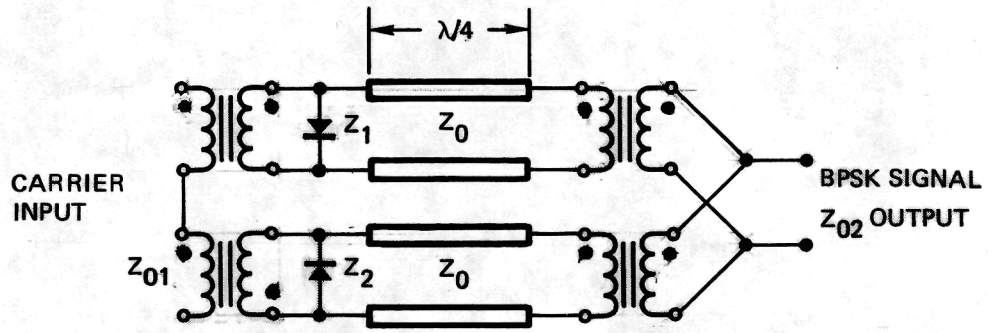
Figure 3-7 shows the fundamental operation of the biphase switch. In this figure, arrows represent the schematic expression of the carrier, i.e., the arrows show the direction of the electric field of the carrier which propagates along the slotline. The 60 GHz signal at the microstrip input is transferred to the slotline via the microstrip-slotline transition. The bias states of the Schottky diodes then determine which path the signal takes as the data alternately switches the Schottky diodes on and off. The signal takes path 1 or path 2 producing a biphase output signal since the direction of the electric field at the output junction is 180° out-of-phase, as shown in Figure 3-7. A second slotline-microstrip transition is used to transfer the modulated 60 GHz modulated signal back to the microstrip medium.



(A) WITH DIODE D_1 SHORT



(B) WITH DIODE D_2 SHORT



(C) EQUIVALENT CIRCUIT

Figure 3-7. Operating Principle of Biphase Switch

3.2.2 Slotline Impedance Calculation

The slotline wavelength and impedance can be computed based on closed form expressions reported by Gupta, Gary and Bahl [4]. The closed form expressions were obtained by curve fitting the results from Cohn's analysis [5]. These expressions have an accuracy of about 2 percent.

In most applications, the following parameters are met (Figure 3-8):

$$9.7 \leq \epsilon_r \leq 20$$

$$0.01 \leq h/\lambda_o \leq (h/\lambda_o)_c$$

where (h/λ_o) is the cutoff value for the TE_{10} surface-wave mode defined by

$$(h/\lambda_o)_c = 0.25/\sqrt{\epsilon_r - 1} \tag{3.2-1}$$

The approximate expressions for wavelength and impedance are given by:

(1) For $0.02 \leq W/h < 0.2$:

$$\lambda_s/\lambda_o = 0.923 - 0.448 \log \epsilon_r + 0.2\, W/h - (0.29\, W/h + 0.047) \log (h/\lambda_o \times 10^2) \tag{3.2-2}$$

$$Z_{os} = 72.62 - 35.19 \log \epsilon_r + 50 \frac{(W/h-0.02)(W/h-0.1)}{W/h} + \log(W/h \times 10^2)[44.28-19.58 \log \epsilon_r] - [0.32 \log \epsilon_r - 0.11 + W/h(1.07 \log \epsilon_r + 1.44)] \cdot (11.4 - 6.07 \log \epsilon_r - h/\lambda_o \times 10^2)^2 \tag{3.2-3}$$

(2) For $0.2 \leq W/h \leq 1.0$

$$\lambda_s/\lambda_o = 0.987 - 0.483 \log \epsilon_r + W/h(0.111 - 0.0022\, \epsilon_r) - (0.121 + 0.094\, W/h - 0.0032\, \epsilon_r) \log (h/\lambda_o \times 10^2) \tag{3.2-4}$$

$$Z_{os} = 113.19 - 53.55 \log \epsilon_r + 1.25\, W/h(114.59 - 51.88 \log \epsilon_r) + 20(W/h - 0.2)(1 - W/h) - [0.15 + 0.23 \log \epsilon_r + W/h(-0.79 + 2.07 \log \epsilon_r)] \cdot [10.25 - 5 \log \epsilon_r + W/h(2.1 - 1.42 \log \epsilon_r) - h/\lambda_o \times 10^2]^2 \tag{3.2-5}$$

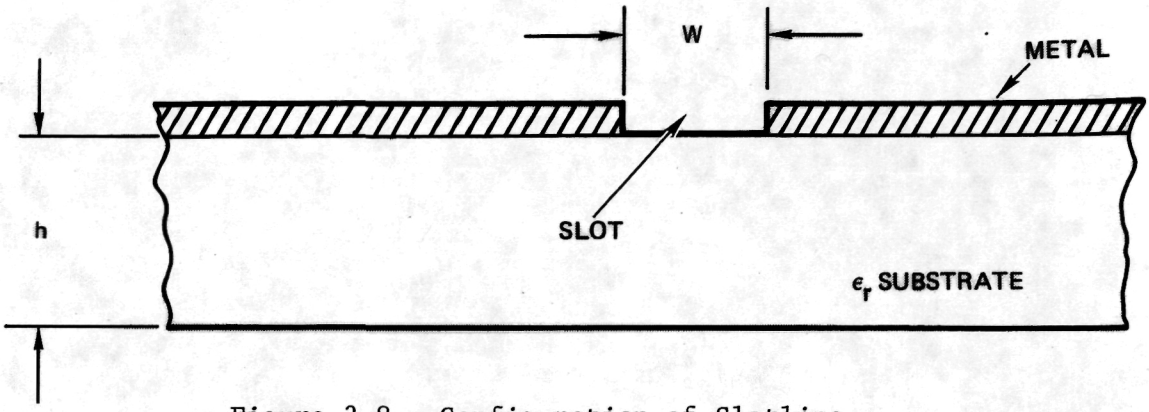


Figure 3-8. Configuration of Slotline

3.2.3 Slotline-to-Microstrip Transition

A microstrip to slotline transition is shown in Figure 3-9. The slotline, which is etched on one side of the substrate, is crossed at a right angle by a microstrip conductor on the opposite side. The microstrip extends about one quarter of a wavelength beyond the slotline and, similarly, the slotline extends about one quarter of a wavelength beyond the microstrip. The microstrip is placed on one side of the substrate and the slotline on the other side. The transition thus makes two-level circuit design possible. An equivalent circuit of this transition is shown in Figure 3-9. The reactance X_{ss} represents the inductance of a shorted slotline and C_{om} is the capacitance of an open microstrip. Z_{os} and Z_{om} are slotline and microstrip impedance, respectively. θ_s and θ_m represent the electrical lengths of the extended portions of the slotline and the microstrip. The value of the transformer ratio, n, is determined from the knowledge of slotline-field components [6].

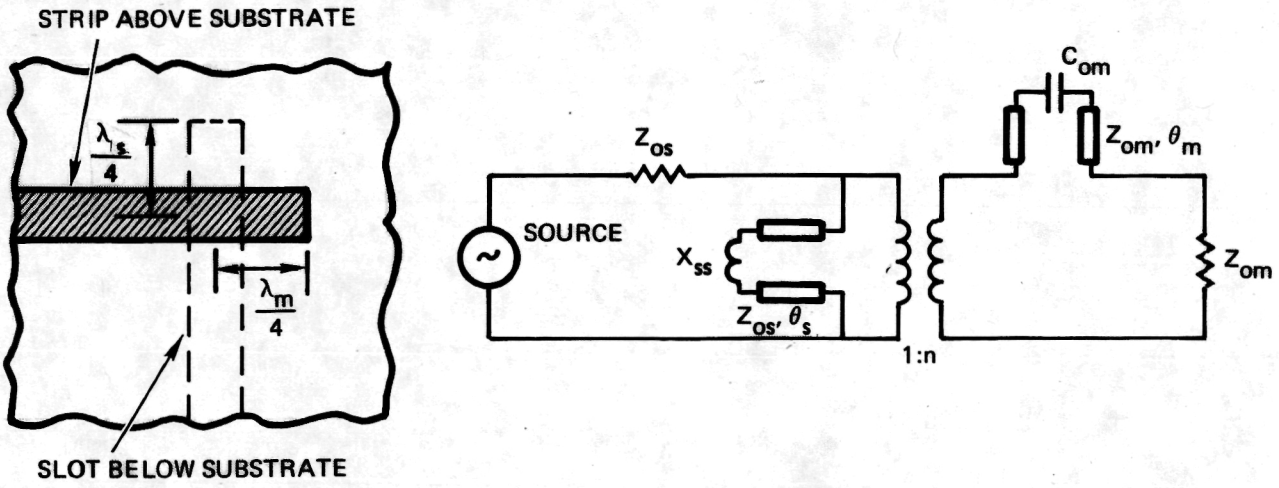


Figure 3-9. Configuration and Equivalent Circuit of a Microstrip-to-Slotline Transition

3.2.4 Shunt and Series Mounted Structure Tradeoff

In the early stages of this program, a tradeoff study between shunt and series mounted structures was conducted. A series mounted biphase switch, as shown in Figure 3-10, was designed and tested. Compared to the shunt-mounted switch (Figure 3-6), the scheme has advantages of simplicity and a possibility of completely eliminating the microstrip-to-stripline transition. The 180° phase difference is introduced by the circular arc spaced between the two diodes. The switching action can be accomplished by selectively shorting one diode or the other.

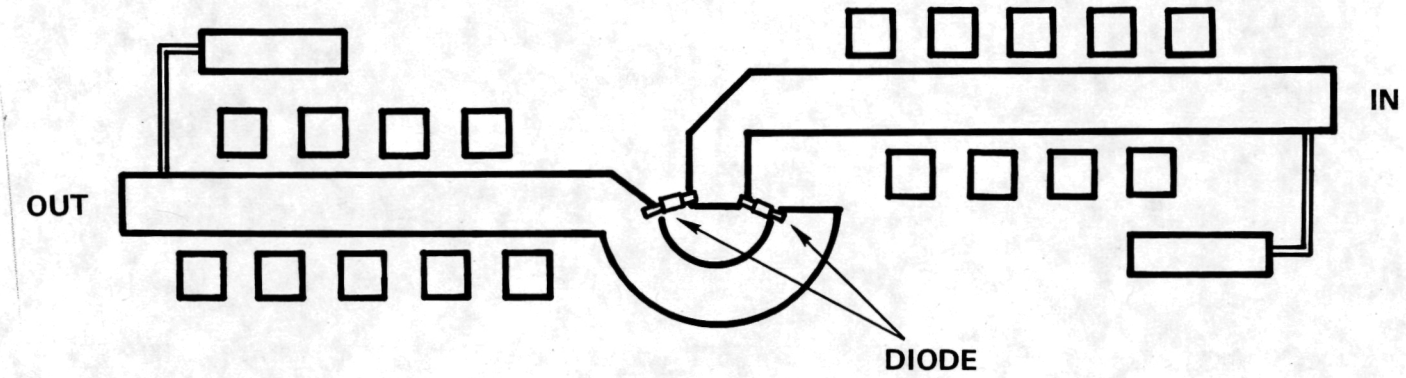


Figure 3-10. Series Mounted Biphase Switch Circuit Layout

The series mounted biphase switch was built at 15 GHz for easier optimization. Insertion loss of 2.5 dB, isolation of 19 dB, and ±2° phase imbalance have been achieved at 15 GHz. After the optimization, the circuit was scaled up to 60 GHz. An insertion loss of about 3 dB was achieved at 60 GHz, but the isolation was too low (around 5 dB).

The low isolation is believed to be due to the high package capacitance associated with the beamlead Schottky-barrier diodes. Figure 3-11 shows the equivalent circuit of a diode. The diode chip is represented by a junction capacitance (C_j), a junction resistance (R_j), and a series resistance (R_s). L_s and C_p represent the package lead inductance and package capacitance, respectively. Neglecting the package parasitics, the insertion loss is given by

$$\alpha_L = 20 \log \left[1 + \frac{R_s}{Z_o} \right] \quad \text{dB} \qquad (3.2\text{-}6)$$

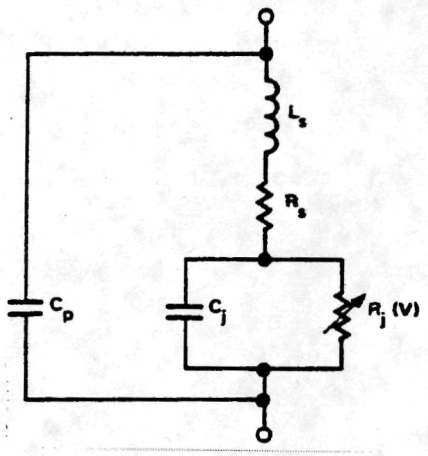


Figure 3-11. Diode Equivalent Circuit

and the isolation is obtained by

$$\alpha_I = 10 \log \left[1 + \left(\frac{1}{4\pi f C_j Z_o}\right)^2\right] \text{ dB} \qquad (3.2\text{-}7)$$

Therefore, the lower the value of R_S and the lower the value of C_j, the lower the insertion loss and higher the isolation.

The Schottky-barrier diodes have typical series resistance of 5 ohms and junction capacitance of 0.05 pF. The calculated insertion loss at 60 GHz is about 0.8 dB and the isolation is 1 dB.

For a shunt-mounted structure, the insertion loss is calculated by

$$\alpha_L = 10 \log [1+(\pi f C_j Z_o)^2] \text{ dB} \qquad (3.2\text{-}8)$$

and the isolation is given by

$$\alpha_I = 20 \log \left(\frac{Z_o}{ZR_j} + 1\right) \text{ dB} \qquad (3.2\text{-}9)$$

The calculated insertion loss at 60 GHz is about 0.8 dB and the isolation is over 15 dB.

Although the above calculations are approximated neglecting the package parasitics, it can be concluded that at 60 GHz the shunt-mounted structure has similar insertion loss compared to the series-mounted structure,

but with much higher isolation. The experimental results confirmed this prediction and the shunt-mounted configuration, as shown in Figure 3-6, was selected as our baseline approach.

3.2.5 Biphase Switch Performance

The shunt-mounted biphase switch was first fabricated at 15 GHz on Duroid 6010 substrate to establish the feasibility. Duroid 6010 was used for its flexibility and high dielectric constant of 10, which is close to that of sapphire. Measurements at 15 GHz indicated an insertion loss of 3 dB and an isolation of 25 dB (Figure 3-12).

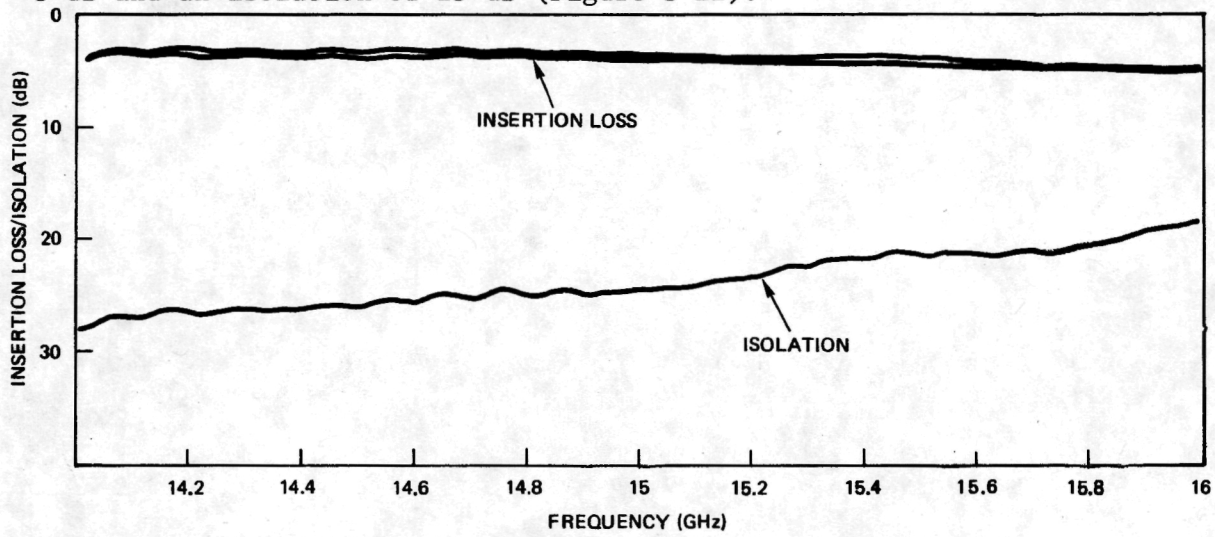
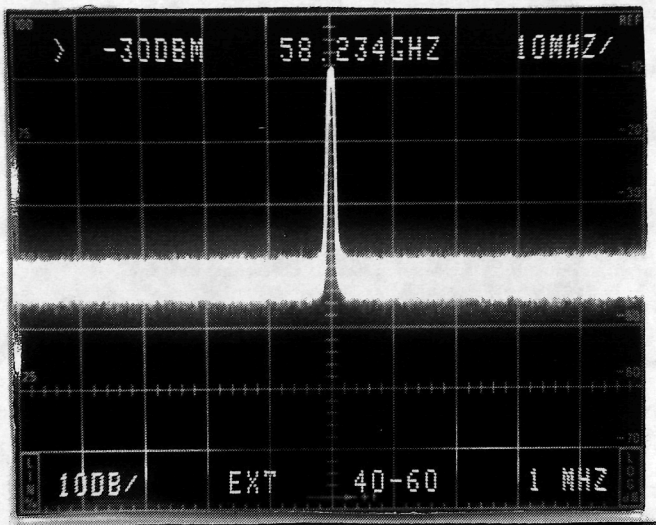


Figure 3-12. Performance of 15 GHz Biphase Switch

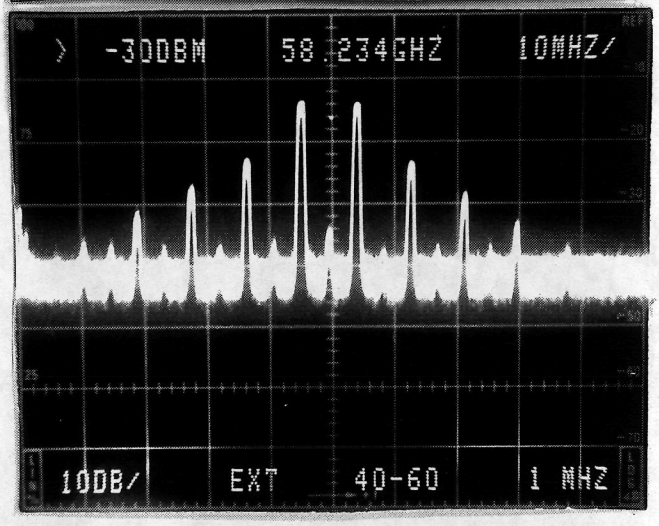
The 15 GHz biphase switch design was then scaled up to 60 GHz. Figure 3-13 shows the performance of this biphase switch. The data shows very good phase and amplitude balance (phase balance less than ±3° and amplitude balance less than ±0.5 dB). The carrier suppression is over 20 dB for the modulated signal. The isolation can be measured by the control of bias level. With one diode "OFF", the leakage from one diode is illustrated in Figure 3-14(a). With both diodes "OFF", the leakage from both diodes is shown in Figure 3-14(b). The isolation from one diode is over 20 dB.

3.2.6 Limitations

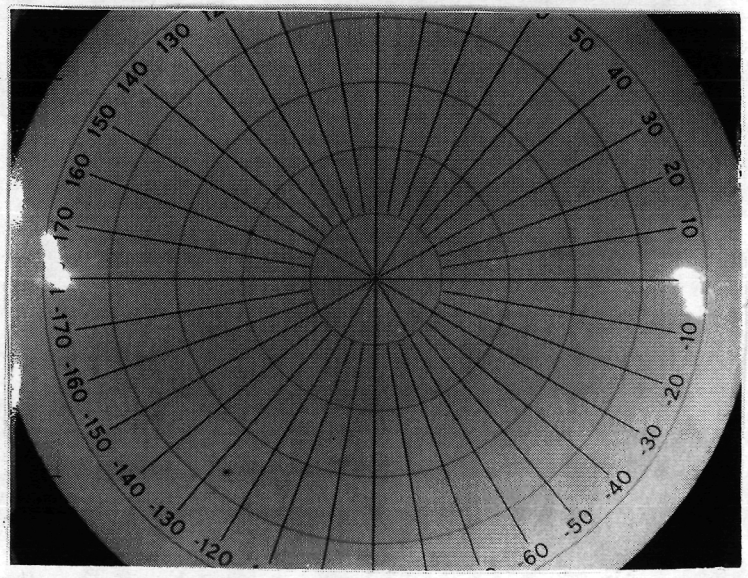
At 60 GHz, the beamlead package dimensions are 40% of a quarter wavelength and the package reactances are high. Figure 3-15 illustrates the diode and slot dimensions. Slight offset of the diodes results in significant phase and amplitude imbalance. To overcome this problem, an



(a)
Unmodulated Carrier

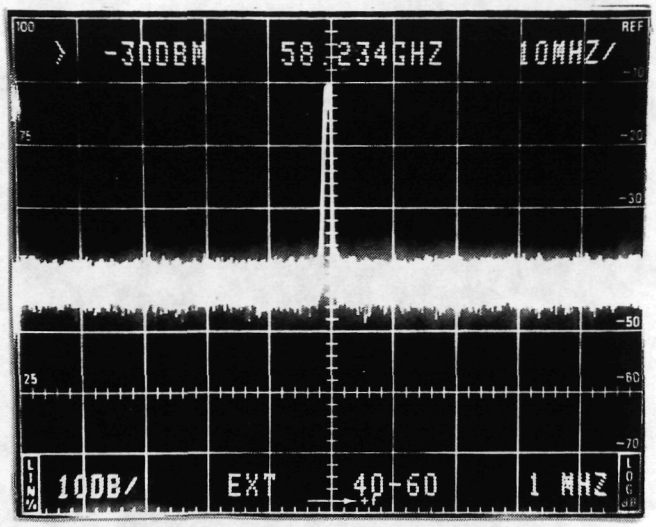


(b)
10 MHz Modulation



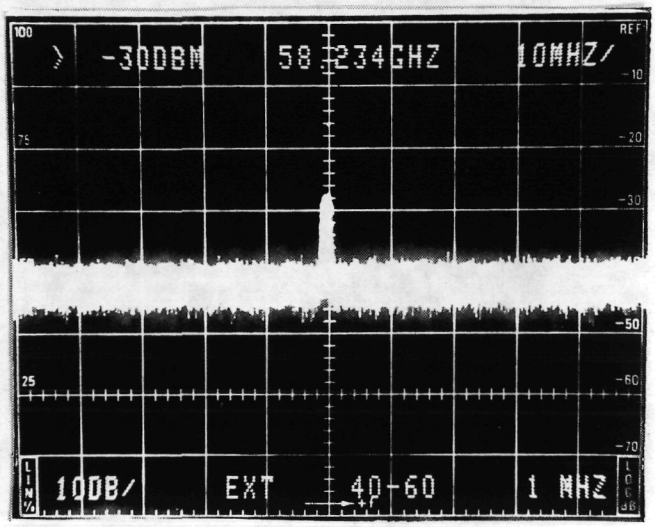
(c)
Biphase States

Figure 3-13. 60 GHz Biphase Switch Performance



Carrier

(a) Output Carrier with One Diode "OFF"



Isolation

(b) Output with Both Diodes "OFF"

Figure 3-14. Biphase Switch Isolation Measurement (Including Leakage from Both Diodes)

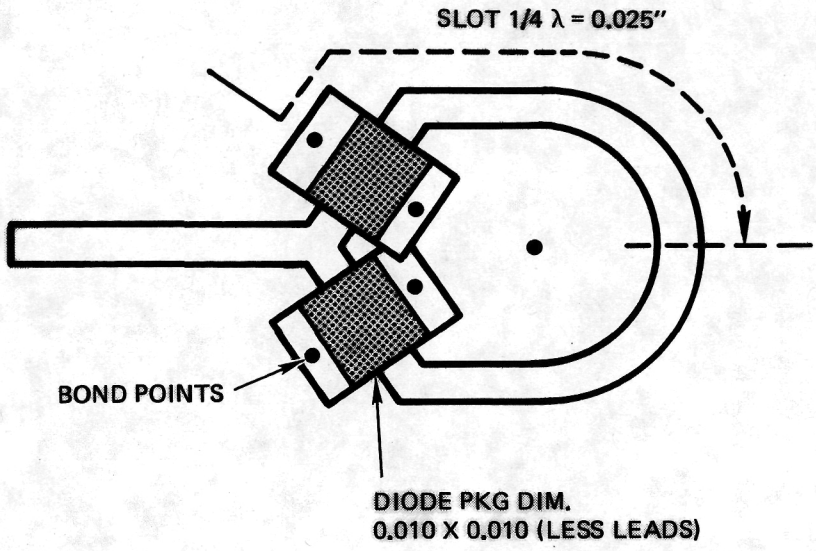


Figure 3-15. Biphase Switch Dimensions

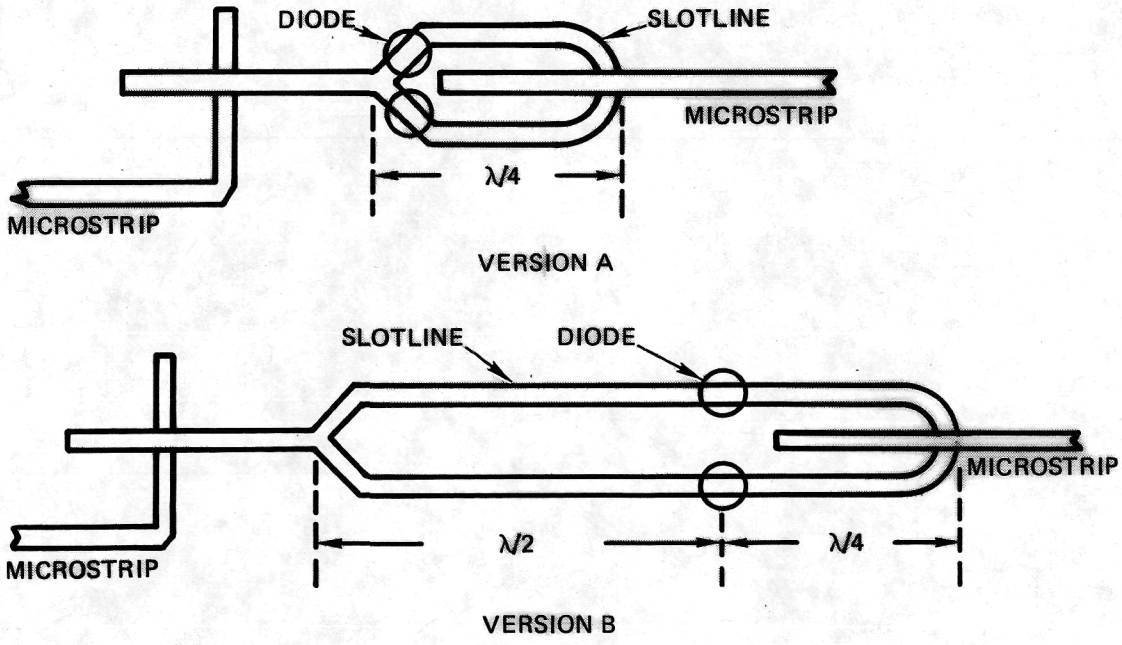


Figure 3-16. Two Different Versions of Biphase Switch

alternative approach (shown on Figure 3-16 as Version B) was investigated. The original scheme is designated as Version A in Figure 3-16. Version B is similar to Version A except that an additional half wavelength is incorporated between the diodes and the switching junction. Experimental results indicated that both versions provided identical insertion loss but phase and amplitude parameters were much more critical to diode placement with Version B.

The ultimate solution to this dimension limitation is to develop a monolithic chip with diodes grown in-situ. In this way, diode bonding can be avoided and accurate positioning of diodes can be achieved.

3.3 MODULATOR FABRICATION

The QPSK modulator was fabricated on a 5-mil thick sapphire substrate with a relative permittivity of 9.6. The substrate material was supplied by both Crystal Systems and Adoph Meller Corporation. To our knowledge, these are the only companies that can polish such thin sapphire substrates, as this is a very difficult task. Very thin substrates tend to curl up when removed from the polishing cap due to surface stresses that build up. (This is sometimes known as "potato chipping.") The substrates as delivered were 1 inch square and 0.005 ± 0.0025 inch thick.

Metallization was applied in-house at TRW. A layer of nickel-chromium (500 Å thick) was deposited as a refractory base layer, followed by 100 μm of gold. The nickel-chromium layer serves two purposes: it enables the gold to adhere to the sapphire and it allows the fabrication of thin film resistors. Nickel-chromium has a significnatly higher resistance than gold, so removing gold metallization forms a resistor. A microwave resistor can be constructed by etching the gold away and exposing the nickel-chromium. Figure 3-17 shows a power divider circuit with the nickel-chromium exposed to form a terminating resistance.

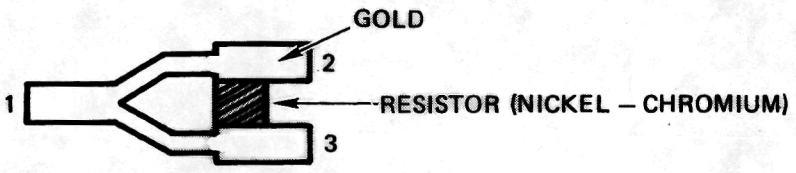


Figure 3-17. Forming of a Resistor on Sapphire Substrate

The complete modulator is contained on a sapphire chip with dimensions of 0.270x0.1x0.005 in. The circuit was created by starting with a 100X tape-up of the designed pattern. At this scale, circuit modifications are easily accomplished, and any dimensional errors are reduced by a factor of 100. This gave a very accurate representation of the circuit pattern on glass to be used for the etching process. The pattern was repeated 12 to 16 times, depending on the width of the circuit, in order to use as much of the sapphire as possible.

The masks were aligned using a Casper mask aligner. A total of four masks is required for each circuit--one mask for each metal on each side. The gold is etched with iodine, and the chrome is removed with HNO_3 and cerium nitrate. The finest lines or gaps that can be etched are 0.001±0.0005 in. This is sufficient for our purposes, as thinner lines have extremely high losses.

The completed substrate is then sawed into individual circuits using a 10-mil diamond saw. Visual inspection is used to select chips with no flaws. Diodes and bond wires are then attached and the completed device is mounted in a suitable housing for test.

3.4 MICROSTRIP-TO-WAVEGUIDE TRANSITION

Since most test equipment is in waveguide form, it is essential to develop a transition from waveguide-to-microstrip line for component testing. The transition was also used for the output port of the QPSK modulator to couple the modulated signal to waveguide. The transition should have low loss and a bandwidth sufficient for the application. In the past, a cosine ridge-taper transition was used for our testing (Figure 3-18). Although

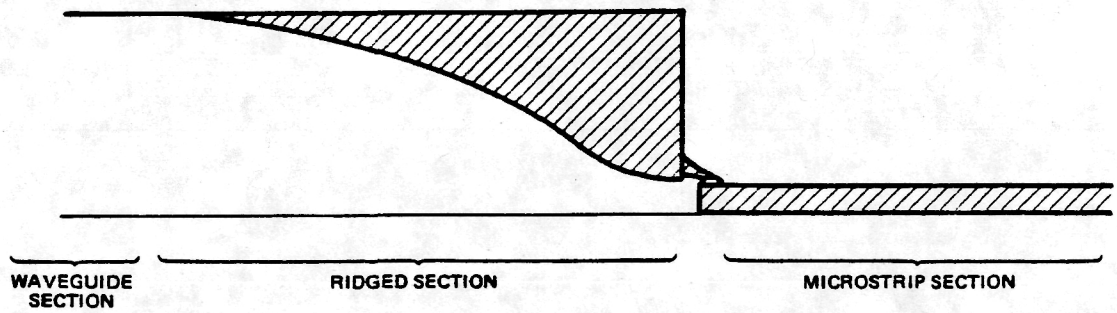


Figure 3-18. Cross-Section of Cosine Ridged Guide-to-Microstrip Transition

the performance of this transition was acceptable, the assembly involved was quite critical because of the small dimensions. Consequently, the results were not reproducible. To overcome this problem, a new type transition using electric probe coupling has been developed. As shown in Figure 3-19, the assembly of this type transition is relatively simple and a sliding short can be used to optimize the performance at a specified frequency.

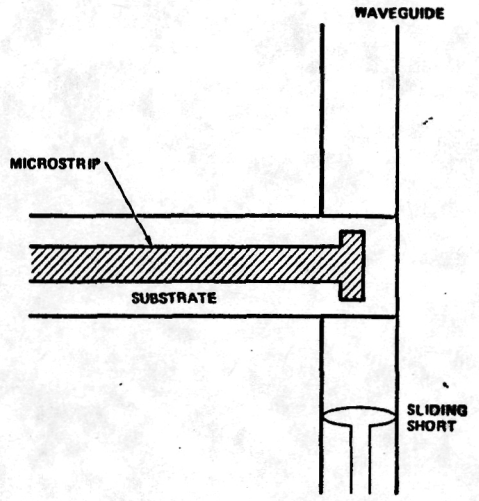


Figure 3-19. Electric Probe Type Microstrip-to-Waveguide Transition

The test fixture for the transition, shown in Figure 3-20, consists of two transitions and a line length of 0.7 in. The performance of this transition is given in Figure 3-21. It can be seen that the total insertion loss, including two transitions and a 0.7 in. microstrip line, is about 1 dB over 58 to 62 GHz. Therefore, the insertion loss per transition is around 0.3 dB. Compared to other types of transitions, the assembly of this type of transition is relatively simple and a sliding short can be used to optimize the performance.

This transition was incorporated at the output port of the QPSK exciter/modulator.

3.5 RF EXCITER/MODULATOR INTEGRATION

The QPSK modulator chip was integrated with the Gunn VCO, subharmonic mixer, directional coupler, and a microstrip-to-waveguide transition to form the RF exciter/modulator module. The modulated 60 GHz output power

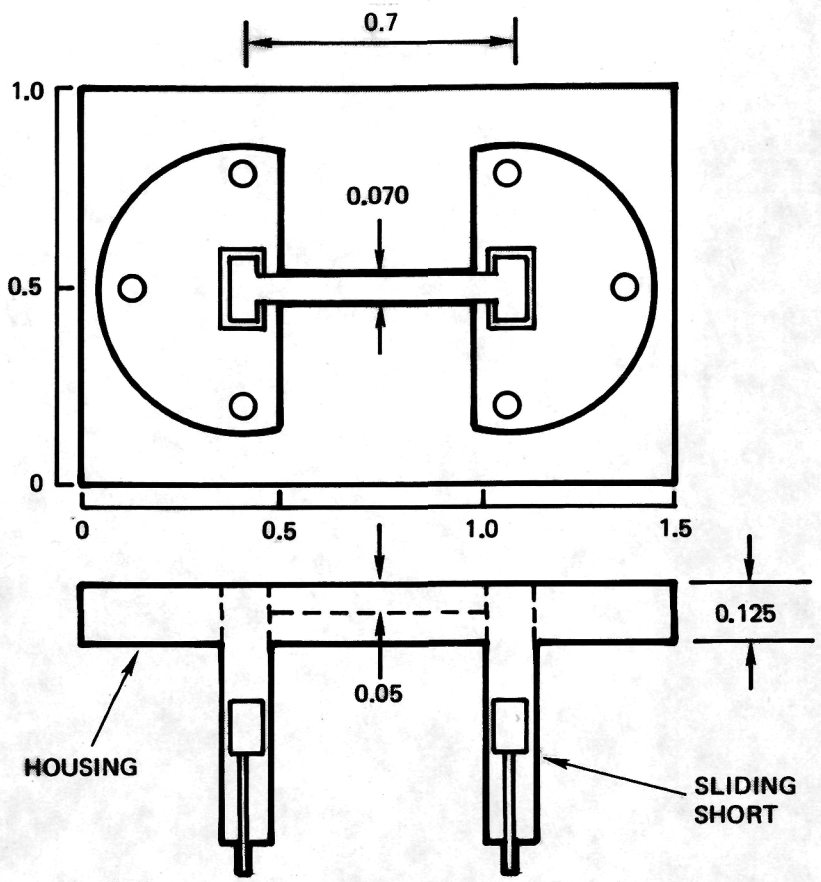


Figure 3-20. Transition Test Fixture (All Dimensions in Inches)

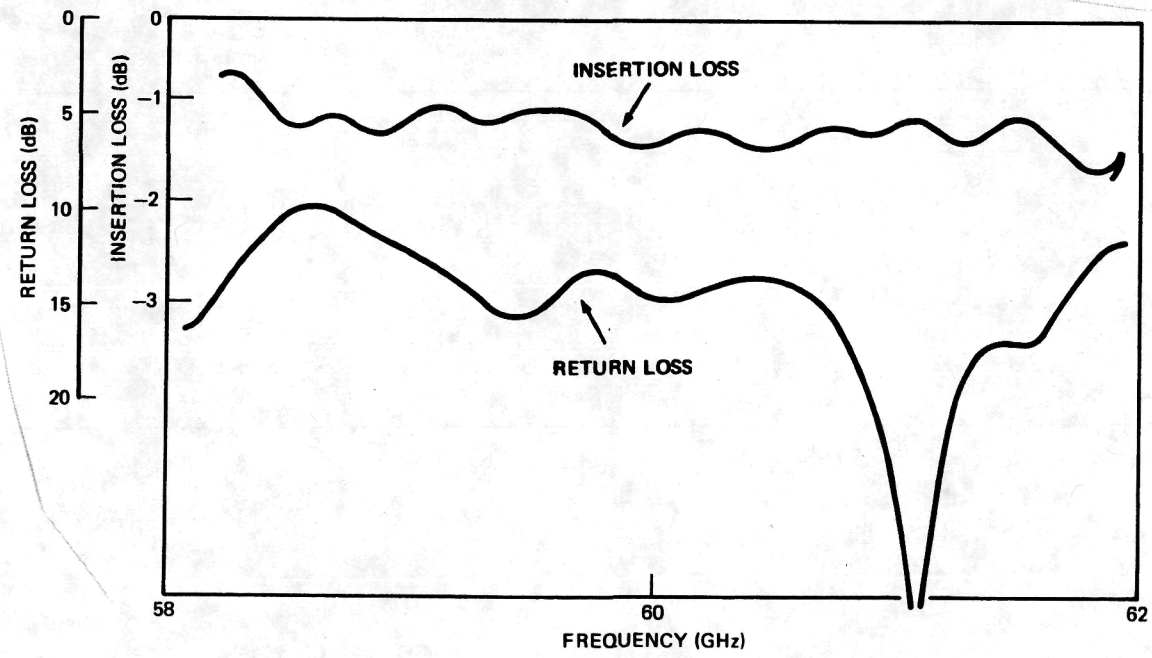


Figure 3-21. Performance of Transition (Including Two Transitions and a 0.7" Microstrip Line)

is coupled to a waveguide through the microstrip-to-waveguide transition. Figure 3-22 shows the circuit board in the RF exciter/modulator module. The unit has a volume of 1.8 x 2.5 x 0.35 in.

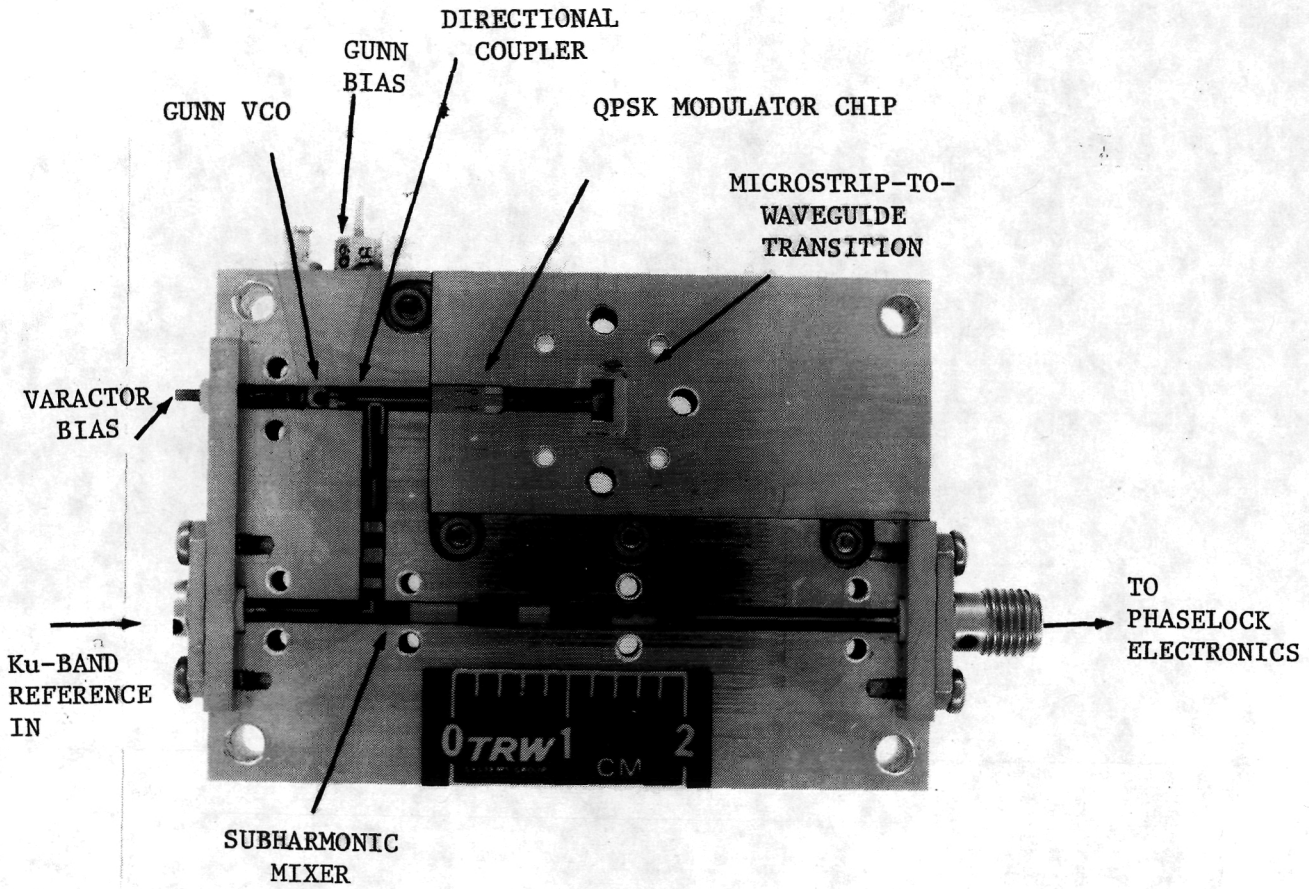


Figure 3-22. RF Exciter/Modulator Module

4. DATA DRIVER DEVELOPMENT

A data driver was required to insure proper data level to the modulator is functional. Although the modulator was designed to achieve 2 gigabits per channel data rate, it is difficult and expensive to test this data rate based on the present technology. A modulator driver with lower data rate was thus developed for testing purposes.

4.1 DATA DRIVER CIRCUIT

As shown in the block diagram of Figure 4-1 and in the schematic diagram of Figure 4-2, the data driver consists of:

- Data buffer, U1, the TRW 1 GHz flip flop.
- Three stages of current gain using 4 pairs of differential switches.
- Positive and negative current sources, Q3, Q17-Q19.
- DC bias/reference circuit including VR1, VR2, Q6, Q7, Q15 and Q16.
- External asymmetry adjustment control circuit, Q4 and Q5, accessed by the output taps A1 and A2.

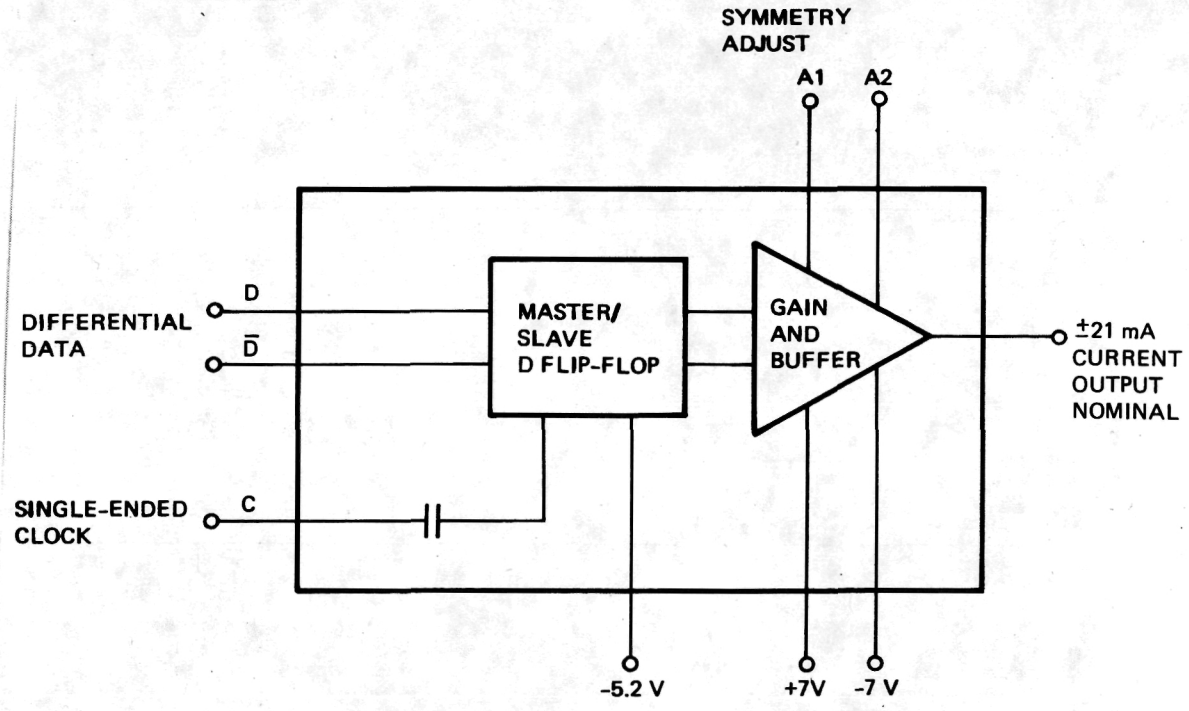
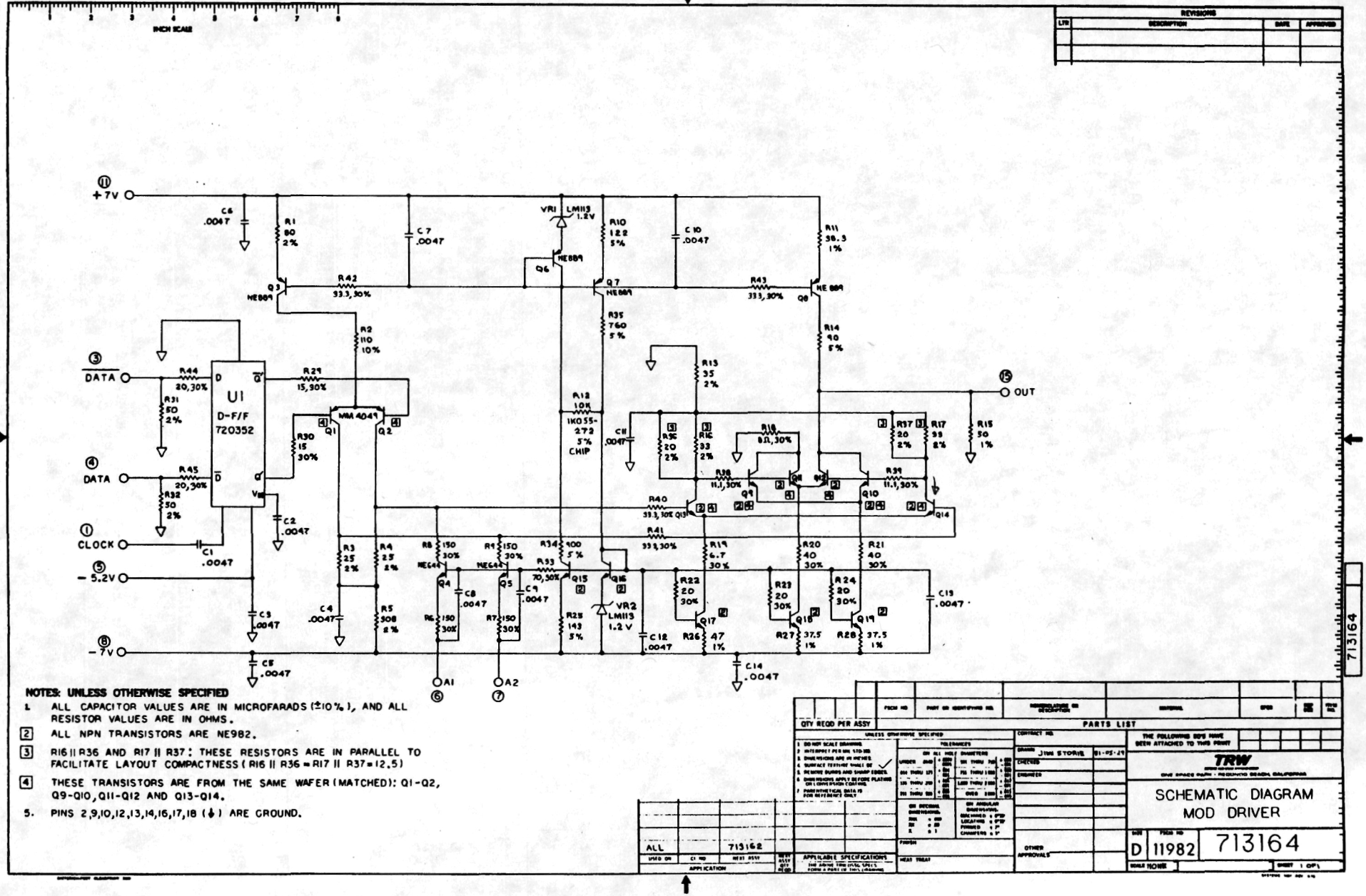


Figure 4-1. Data Driver Block Diagram



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITOR VALUES ARE IN MICROFARADS (±10%), AND ALL RESISTOR VALUES ARE IN OHMS.
2. ALL NPN TRANSISTORS ARE NE982.
3. R16 || R36 AND R17 || R37: THESE RESISTORS ARE IN PARALLEL TO FACILITATE LAYOUT COMPACTNESS (R16 || R36 ≈ R17 || R37 = 12.5)
4. THESE TRANSISTORS ARE FROM THE SAME WAFER (MATCHED): Q1-Q2, Q9-Q10, Q11-Q12 AND Q13-Q14.
5. PINS 2,9,10,12,13,14,16,17,18 (⏚) ARE GROUND.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

713164

QTY REQD PER ASSY | PARTS LIST

THE FOLLOWING DFS HAVE BEEN ATTACHED TO THIS PRINT

TRW

SCHEMATIC DIAGRAM
MOD DRIVER

SIZE	FSCM NO	
D	11982	713164

SCALE NONE | SHEET 1 OF 1

ALL	713162
USED ON	CI NO
APPLICATION	NEXT ASSY

APPLICABLE SPECIFICATIONS

Figure 4-2. Detailed Circuit Diagram

The input buffer, U1, provides synchronous timing and data storage capability. Three cascaded stages of differential pairs follow the buffer. Q1 and Q2 comprise the first pair, and Q13 and Q14 comprise the second pair. The third stage, two parallel pairs, Q9 and Q10 in parallel with Q11 and Q12, enable 60 mA of current to switch at subnanosecond speeds. Two pairs were used in parallel to take advantage of their maximum bandwidth when biased at 30 mA. 30 mA is obtained from the output by the constant current source Q8. During the data low logic state, Q10 and Q12 sink a total of 60 mA. The composite result during this state is that 30 mA are sunk from the 50 ohm back terminating resistor, R15, in parallel with the modulator load.

The separate positive current source, Q3, and negative current sources, Q17-Q19, are used because of the relatively large amounts of current being switched. The DC bias/voltage reference circuit provides tightly regulated, temperature compensated reference voltages for the current sources and for the output transistor, Q8, and it improves power supply rejection.

Q4 and Q5 enable one to externally adjust the symmetry of the output waveform. Q4 and Q5 collector currents, adjusted by external resistors on the A1 and A2 pins, rechannel current from the collectors of Q2 and Q1, respectively.

The output current is set by actively laser trimming resistors R11, R27 and R28.

Figure 4-3 is a photograph of the data driver whose dimensions are 1.5 x 2.5 x 0.55 in.

4.2 DATA DRIVER TESTING

The test setup is shown in Figure 4-4. The ECL streams are generated by a Tau-Tron data generator. Resistors were used to simulate the diodes. Test conditions are as follow:

Clock Rate: 500 MHz

Data Rate: 500 MBPS

Output current levels have been increased from ±10 mA to ±20 mA. The 20 mA level reduces the biphase switch insertion loss by 1 to 2 dB. Figure 4-5 shows the output data stream. Rise time was measured to be less than 650 ps, as shown in Figure 4-6.

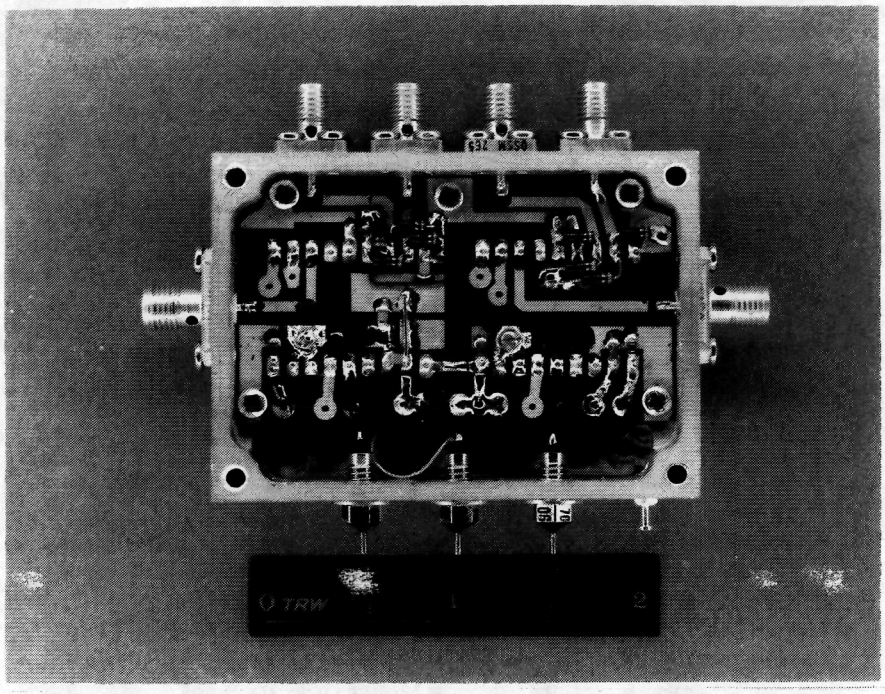


Figure 4-3. Photograph of Data Driver

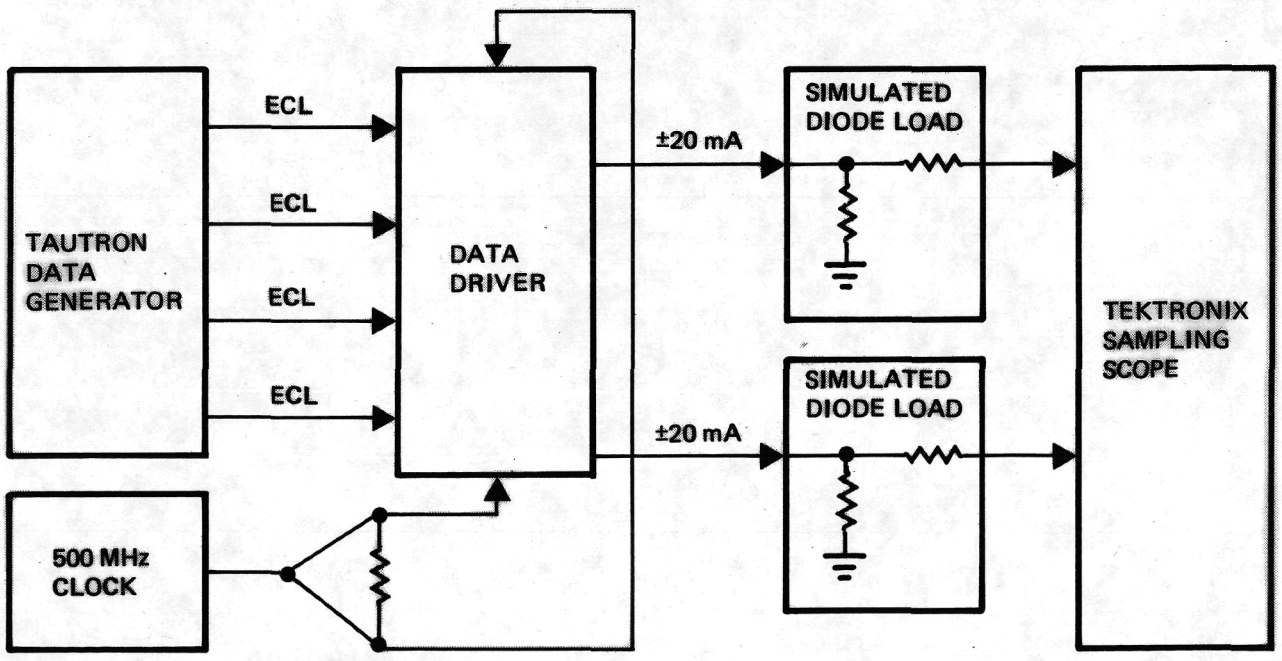


Figure 4-4. Test Setup for Data Driver

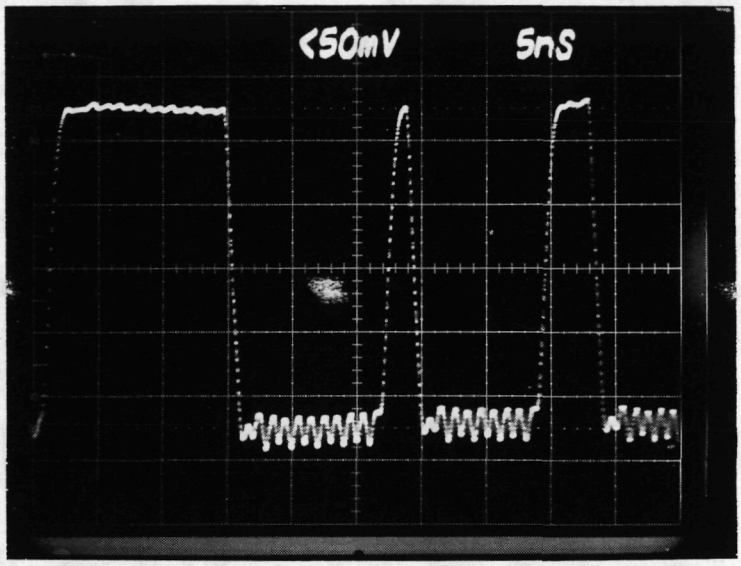
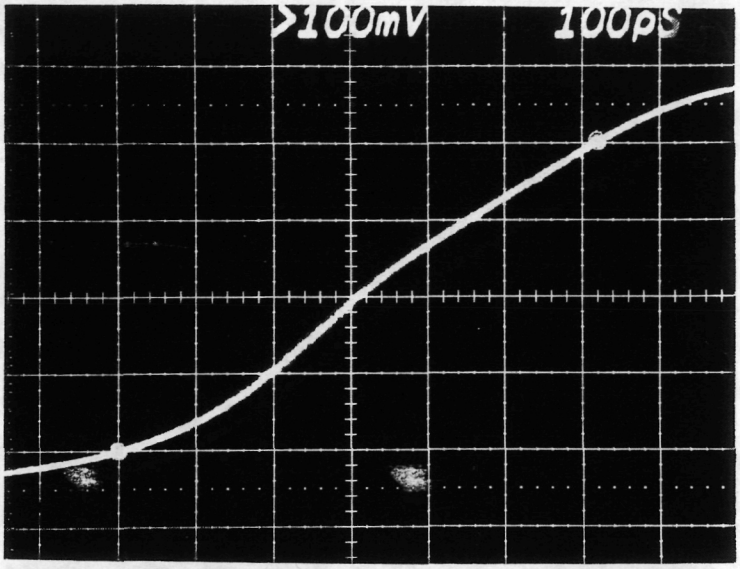
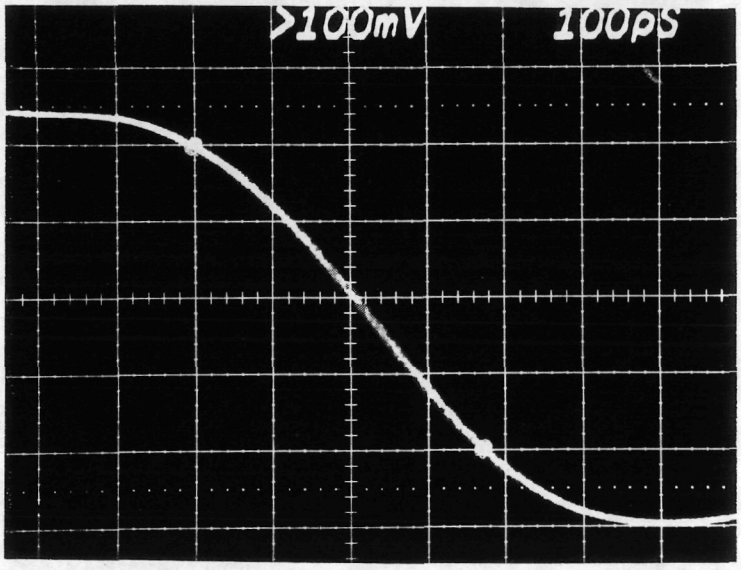


Figure 4-5. Output Data Stream from Data Driver (High Voltage = State "1", Low Voltage = State "0")



RISE TIME



FALL TIME

Figure 4-6. Rise and Fall Time Measurements of the Data Driver at Repetition Rate of 250 MHz

5. INTEGRATION AND PACKAGING

5.1 EXCITER/MODULATOR INTEGRATION

Figure 5-1 is a detailed circuit block diagram for the exciter/modulator. It consists of four modules: RF exciter/modulator module, Ku-band reference source, phaselock electronics, and data driver. The RF exciter/modulator module consists of three subassemblies: exciter subassembly, modulator subassembly and microstrip-to-waveguide transition. The circuits in these modules and subassemblies are:

- RF Exciter/Modulator Module
  - Exciter Subassembly
    - Gunn VCO
    - Directional Coupler
    - Subharmonic Mixer
  - Modulator Subassembly
    - Two Microstrip-to-Slotline Transitions
    - Power Splitter
    - 90 degree Phase Shifter
    - Two Biphase Switches
    - Power Combiner
  - Microstrip-to-Waveguide Transition
- Ku-Band Source Module
  - 2.06896 GHz Stable Crystal-Controlled Source
  - 2.06896 GHz Amplifier and Reference Coupler
  - 2.06896 to 14.4828 GHz Multiplier (X7)
  - Power Regulators
- Phaselock Electronics Module
  - S-Band Circuit and Phase Detector
  - Loop Filter
  - Acquisition Circuits
- Data Driver
  - Data Buffer
  - D-Type Flip-Flop
  - Current Amplifier
  - Current Sources
  - Bias Circuits

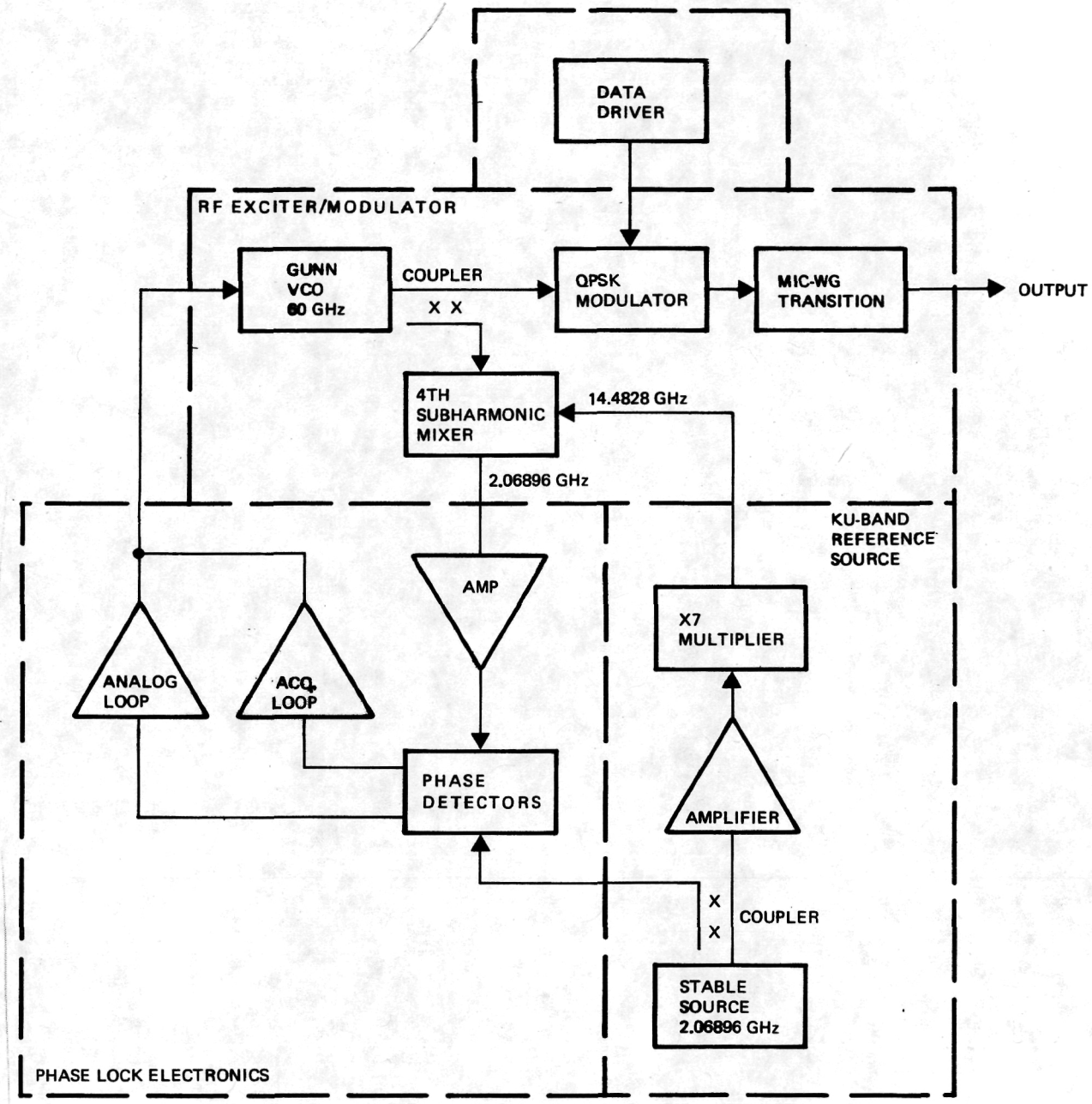


Figure 5-1. Detailed Block Diagram for Exciter/Modulator

The modular approach facilitates testing, measurement, and integration. The module interface chosen provides convenient noncritical test points and allows each module to be optimized separately.

5.2 MECHANICAL DESIGN AND PACKAGING

The mechanical design is a modular concept with the various circuits housed in aluminum modules.

Four modules make up the complete QPSK exciter/modulator (Figure 5-2). The mechanical configurations of these modules and the final packaging are shown in Figure 5-3 and summarized below.

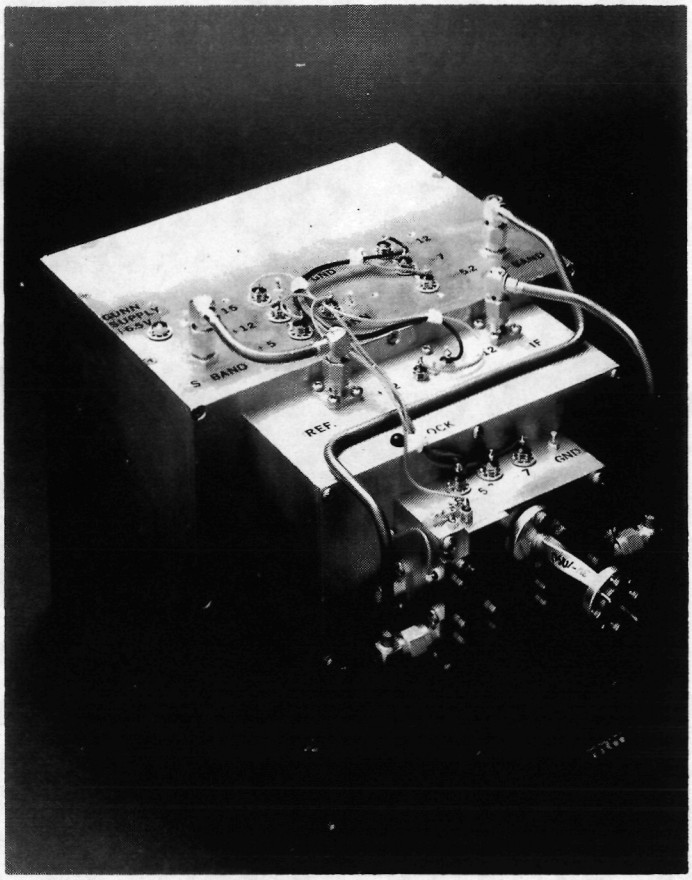


Figure 5-2. Complete QPSK Exciter/Modulator with Associated Phaselock Electronics

5.2.1 RF Exciter/Modulator Module

The RF exciter/modulator module consists of a Gunn VCO, directional coupler, subharmonic mixer, and QPSK modulator chip integrated into a housing measuring 1.8 x 2.5 x 0.35 in. A microstrip-to-waveguide transition was connected to the QPSK modulator output port.

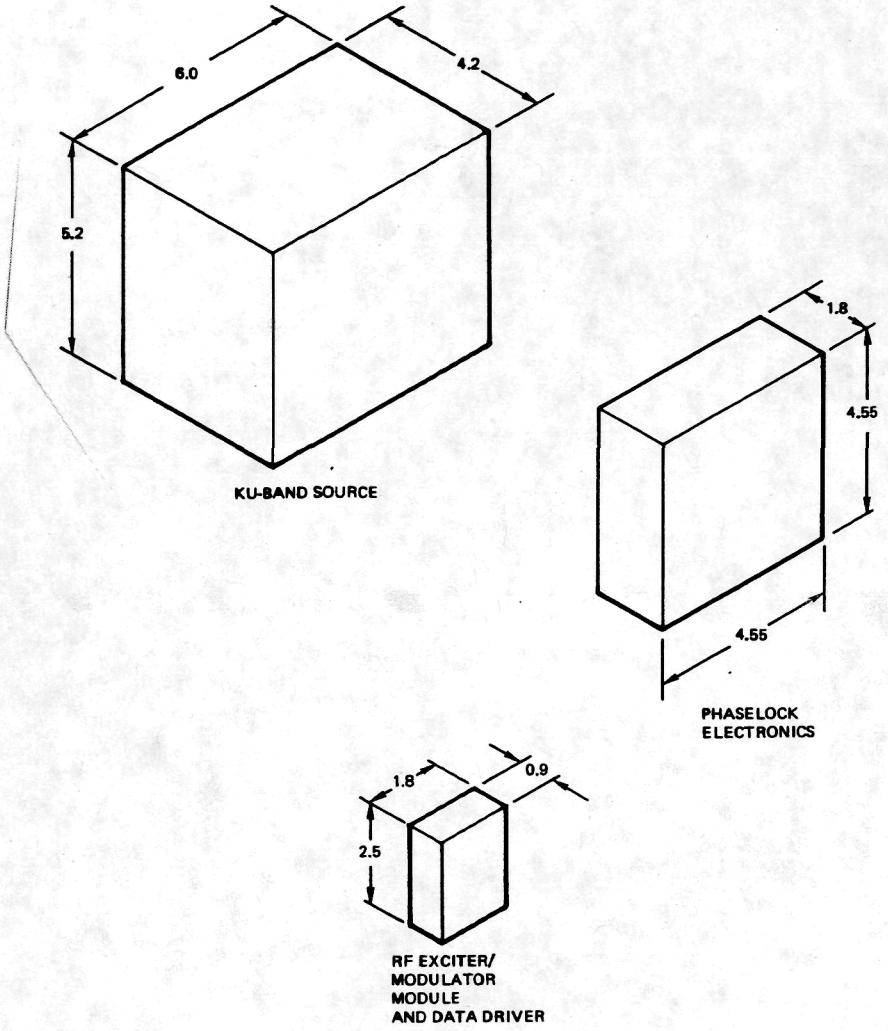


Figure 5-3. Mechanical Layout of QPSK Exciter/Modulator

5.2.2 Ku-Band Source Module

The Ku-band reference Source consists of a 2.06896 GHz stable source, amplifier, the X7 multiplier, and power regulators. These items are housed in a 4.2 x 5.2 x 6.0 in. housing.

5.2.3 Phaselock Electronics Module

The phaselock electronics module contains RF amplifier, phase detector, loop filter, and acquisition electronics. The housing dimensions for this module are 4.55 x 4.55 x 1.8 in.

5.2.4 Data Driver Module

The data driver housing consists of data buffer and storage, current sources and amplifier. The housing dimensions are 1.8 x 2.5 x 0.55 in.

6. EXCITER/MODULATOR TESTING

The critical measurements to be made on the exciter/modulator assembly include static and dynamic tests. The static tests consist of phase and amplitude measurements, insertion loss and return loss measurements. The dynamic tests consist of bit error rate (BER) measurements, eye pattern and data spectrum measurements.

6.1 PHASE AND AMPLITUDE MEASUREMENTS

A 60 GHz network analyzer was modified to measure S_{21} for phase and amplitude balance testing. The network analyzer was originally designed to measure S_{22} and S_{11} only, but inserting the device under test (DUT) in the test arm and shorting the test port allowed transmission phase and amplitude to be measured. The QPSK data inputs are digitally stepped through the four states with a bias source.

The analyzer mainframe has a slow rise time. Therefore, the step frequency must be low enough for the analyzer to track the step rate. The step rate used was 1 kHz. The network analyzer schematic is shown in Figure 6-1.

Several 60 GHz QPSK chips were fabricated and tested with varying results. Diode positioning and bonding techniques were critical factors in obtaining optimum performance. This is due to the large physical size

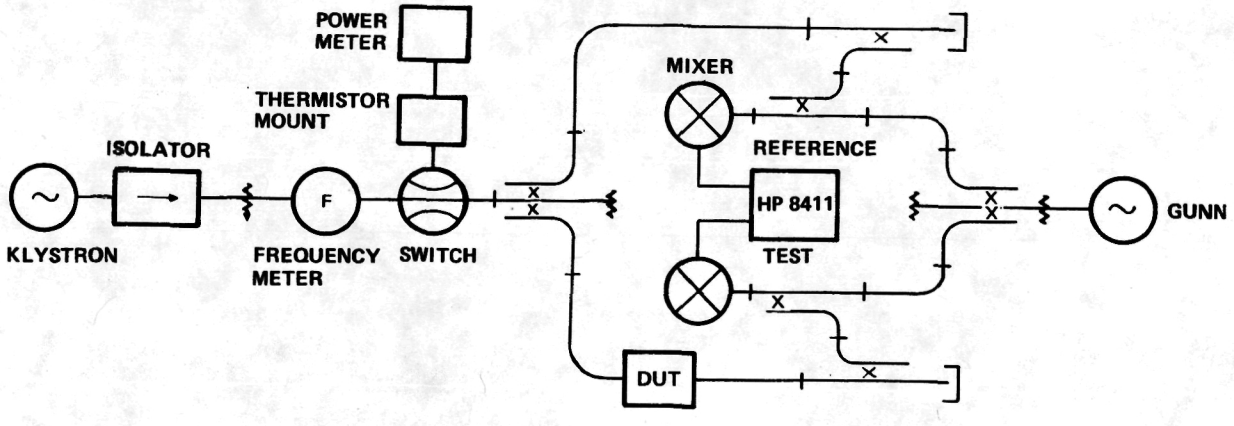
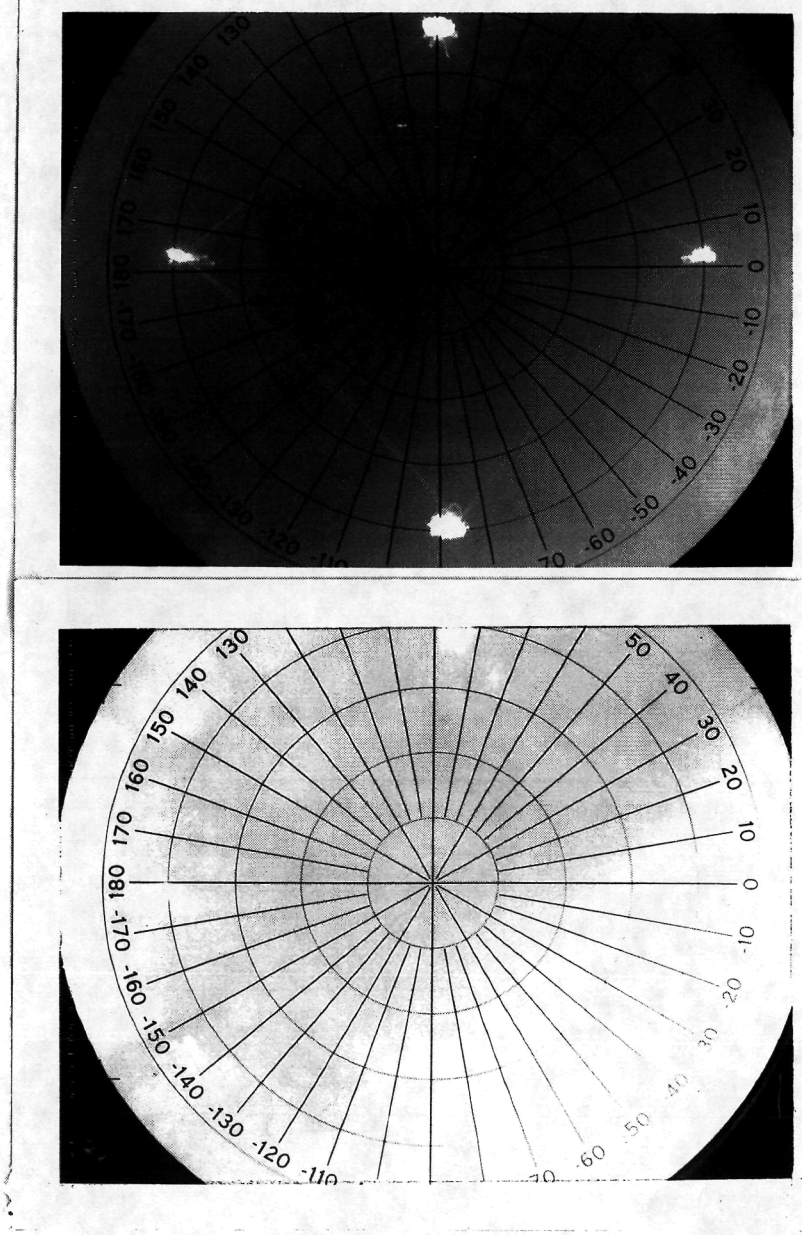


Figure 6-1. 60 GHz Network Analyzer

of the beamlead diodes in relation to a quarter wavelength in slotline as discussed in Section 3. Figure 6-2 shows the phase and amplitude measurements. A phase imbalance of less than ±3° and an amplitude imbalance of 0.5 dB was achieved. These results have met the major program goals.



QPSK CHIP #1

QPSK CHIP #4

Figure 6-2. Phase and Amplitude Measurements for Two Different QPSK Modulator Chips

6.2 INSERTION LOSS AND RETURN LOSS MEASUREMENTS

The network analyzer, as described above, gives absolute insertion loss of the device as well as the relative loss for each phase state. Insertion loss and return loss were measured from 58 GHz to 62 GHz. An insertion loss of 13.5 dB for the modulator and transition was achieved at 60 GHz and varied approximately 1.5 dB across the 4 GHz measurement bandwidth. Return loss at 60 GHz is 13 dB for the input port and 9.5 dB for the output port. The return loss is quite flat across the 4 GHz measurement bandwidth. Figures 6-3 and 6-4 show the insertion loss and return loss plots vs. frequency.

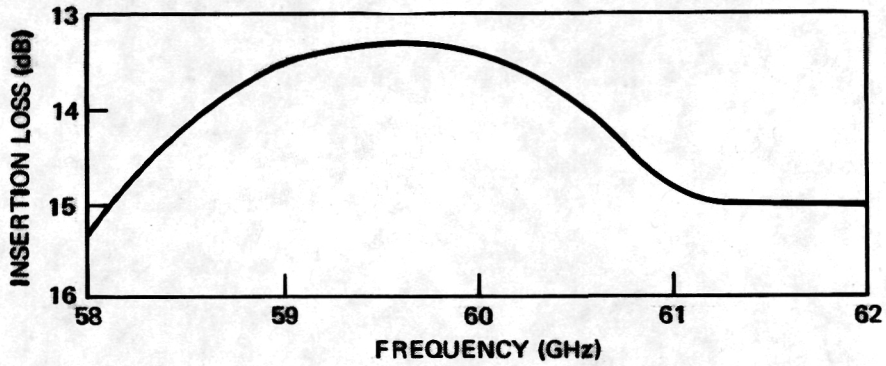


Figure 6-3. QPSK Modulator Insertion Loss Measurement

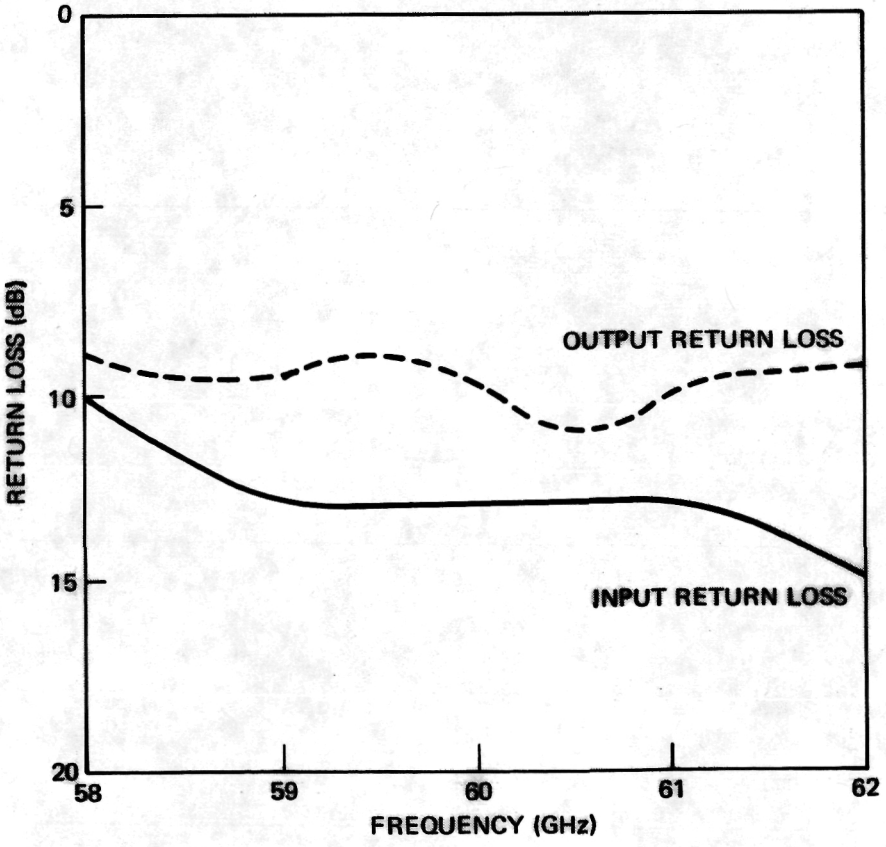


Figure 6-4. QPSK Modulator Return Loss Measurement

With this insertion loss, the output power from the exciter/modulator is about -2 dBm.

6.3 BIT ERROR RATE MEASUREMENT

6.3.1 Bit Error Rate Test Setup

Bit error rate measurements were accomplished with the test set configured as shown in Figure 6-5.

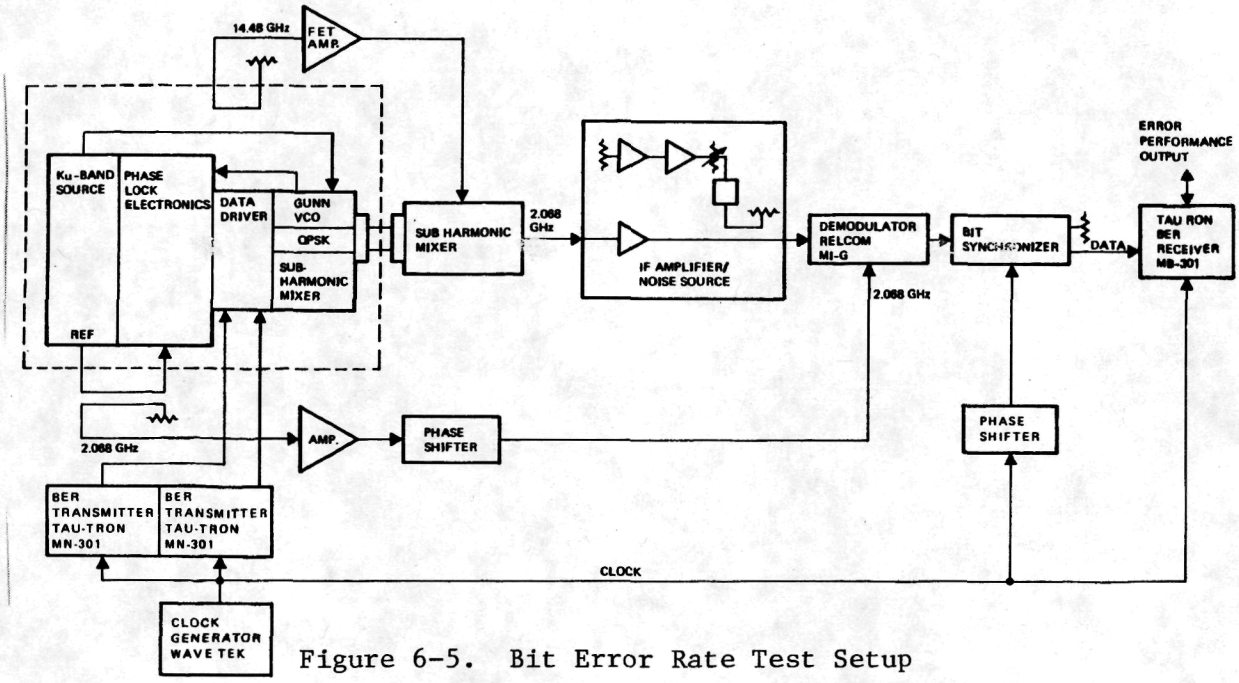


Figure 6-5. Bit Error Rate Test Setup

The V-band integrated QPSK modulator (DUT) is shown within the dotted lines. The blocks outside of the dotted lines make up the BER test set, which functions as follows.

Coherent Downconversion

The 60 GHz QPSK modulated signal is coherently downconverted to 2.068 GHz with a subharmonic mixer. Coherent LO drive was obtained by sampling and amplifying the 14.48 GHz signals from the Ku-band source. The resulting 2.068 GHz signal is then applied to the IF amplifier/noise source.

IF Amplifier/Noise Source

This module amplifies the 2.068 GHz IF signal and provides a noise source with a calibrated output level with a noise bandwidth of 650 MHz. The IF signal and the noise source are then combined with a directional

coupler. A calibrated step attenuator at the noise source output provides adjustment of the signal-to-noise ratio (E_b/N_o). The resulting signal plus noise is then applied to the demodulator.

Demodulator

The demodulator consists of a Relcom M1-G mixer. Coherent LO drive is obtained by sampling the 2.068 GHz reference signal. The sampled signal is amplified and passed through an adjustable phase shifter for control of the demodulation angle. The demodulated output is then applied to the Bit synchronizer.

Bit Synchronizer

The demodulated QPSK signal is passed through the lowpass filter selected to optimize the BER measurement. The decision circuit is a type D flip-flop circuit. Clocking is achieved by connecting directly to the clock generator. A variable phase shifter provides precise adjustment of the clock phase. The bit synchronizer data output represents the demodulated QPSK signal and is applied to the MB-301 receiver to evaluate the BER performance.

MB-301 Receiver

The MB-301 UHF bit error rate test receiver, when used with the MN-301 transmitter, allows error rate measurements to be made over the frequency range of 1 MHz to 325 MHz. The MB-301 has selectable code lengths of 127 bits per frame and 32,767 bits per frame and is driven from an external clock source. The BER is counted and directly displayed on a 4-digit LED display.

6.3.2 Bit Error Rate Testing

Error performance measurements were made with the Tau-Tron MN-301 BER test transmitters and a Tau-Tron MB-301 BER receiver. Two MN-301 BER transmitters were used to drive the QPSK modulator. The MN-301 BER transmitter provides a selectable length pseudorandom data code at rates to 325 MHz. Code lengths of either 127 bits per frame or 32,767 bits per frame may be chosen via a front panel switch.

Bit error rate tests were carried out using the following format:

Mode-Staggered QPSK
Data Rate Per Channel - 325 MBPS
Clock - 325 MHz
System Data Rate - 650 MBPS
Word Length - 2^7-1 Bits

A problem was encountered during BER testing. Because the output port of the 60 GHz Gunn VCO is directly coupled to the QPSK modulator, the Gunn VCO is thus sensitive to the loading effects caused by the switching action of the modulator. These loading effects produce phase shifts in the Gunn output signal perturbing the phase lock loop. These effects are detrimental to BER testing, and were very pronounced when using a long code sequence (2^{15}-1 Bits). These loading effects degrade the performance of communication systems and can be eliminated on future designs by developing a 60 GHz microstrip isolator and inserting it between the Gunn VCO and the QPSK modulator.

Because of the above limitations, all BER tests were conducted using the short code sequence (2^7-1 Bits).

BER measurements were made with E_b/N_o range varying from 7 to 14 dB. The results are plotted in Figure 6-6. Shown are the theoretical curve and experimental results for two channels. It can be seen that the data diverges from the theoretical curve as the signal-to-noise ratio improved. This divergence is caused by the sensitivity of the Gunn VCO loading to the modulator switching action, as previously mentioned.

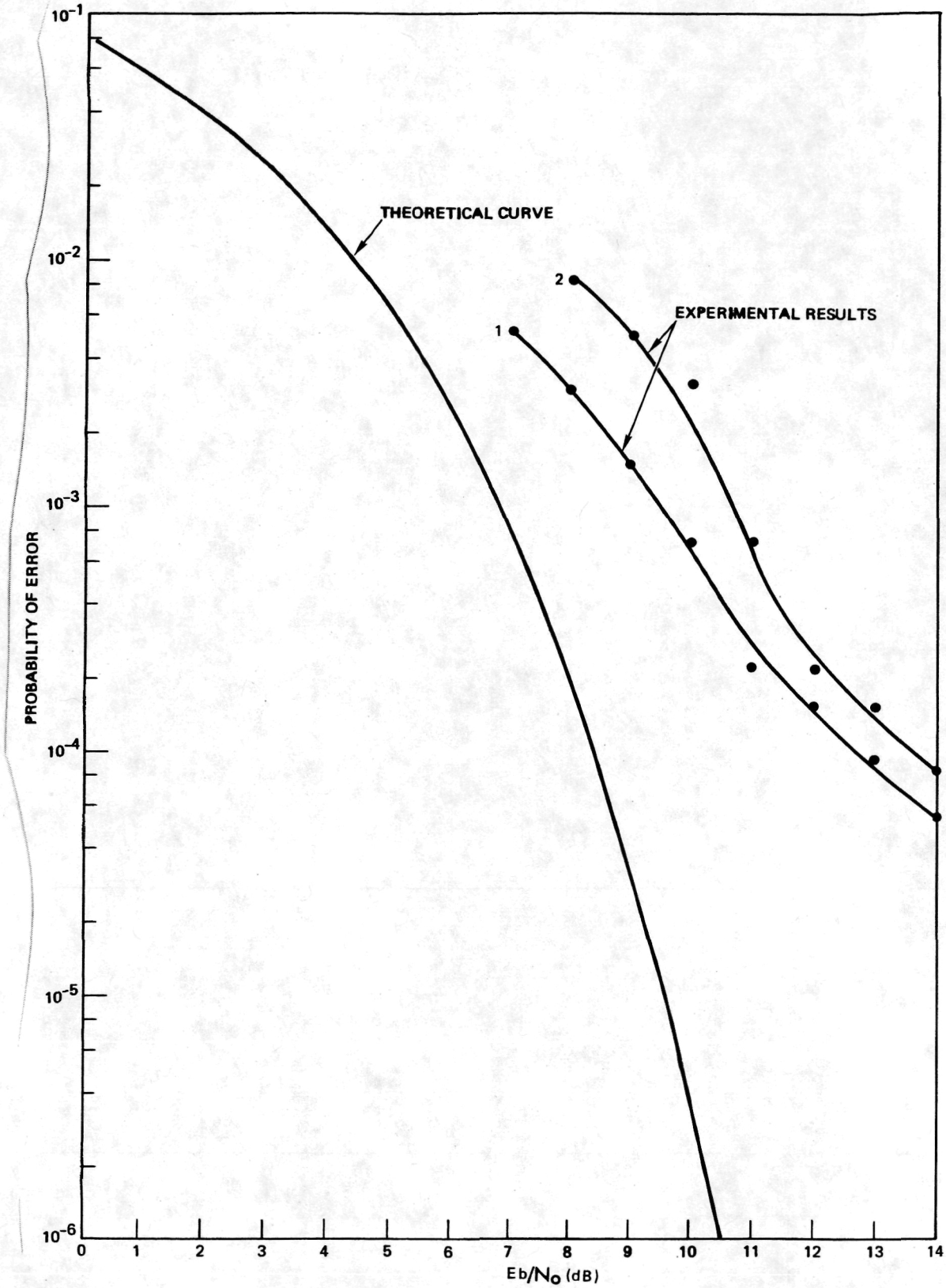


Figure 6-6. Bit Error Rate Measurement Data

6.4 DEMODULATED SPECTRUM AND EYE PATTERN

Figure 6-7 shows the spectrum of an unmodulated signal and Figure 6-8 shows that of a modulated signal. The spectrum is a result of modulating both the I and Q channels with the Tau-Tron BER test transmitters using the short code sequence (2^7-1 bits). The output spectrum was viewed directly with a V-band spectrum analyzer.

Figure 6-9 compares the modulating waveform with the demodulated output. The modulating waveform was observed at the BER transmitter output. The demodulated output signal was observed at the bit synchronizer output. An external delay was used in conjunction with the oscilloscope delay to allow a direct comparison of the modulating waveform and the demodulated output.

Figure 6-10 shows the eye pattern as viewed at the bit synchronizer.

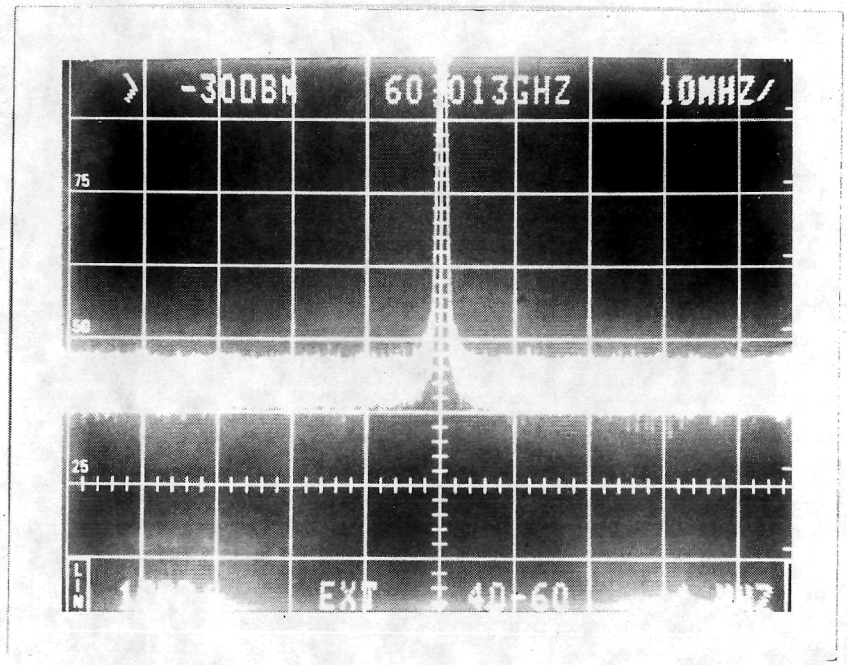


Figure 6-7. Spectrum of Unmodulated Signal

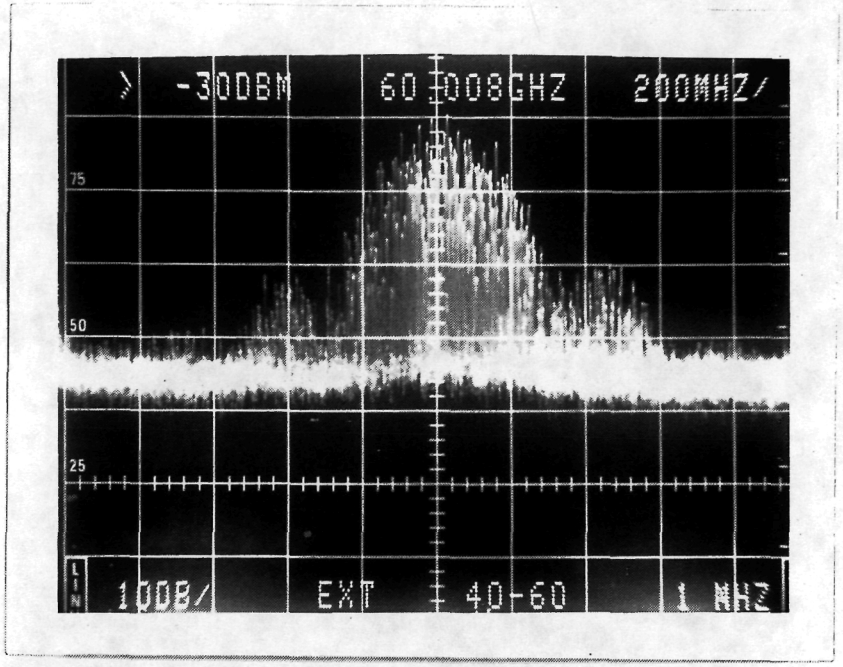


Figure 6-8. Spectrum of Modulated Signal

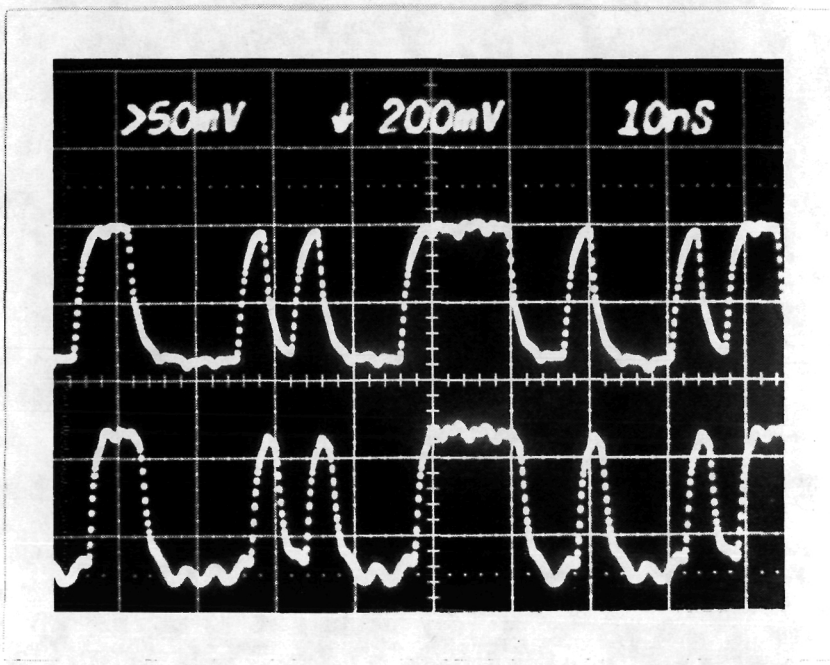


Figure 6-9. QPSK Waveforms. Top trace is modulating signal, bottom trace is demodulated output.

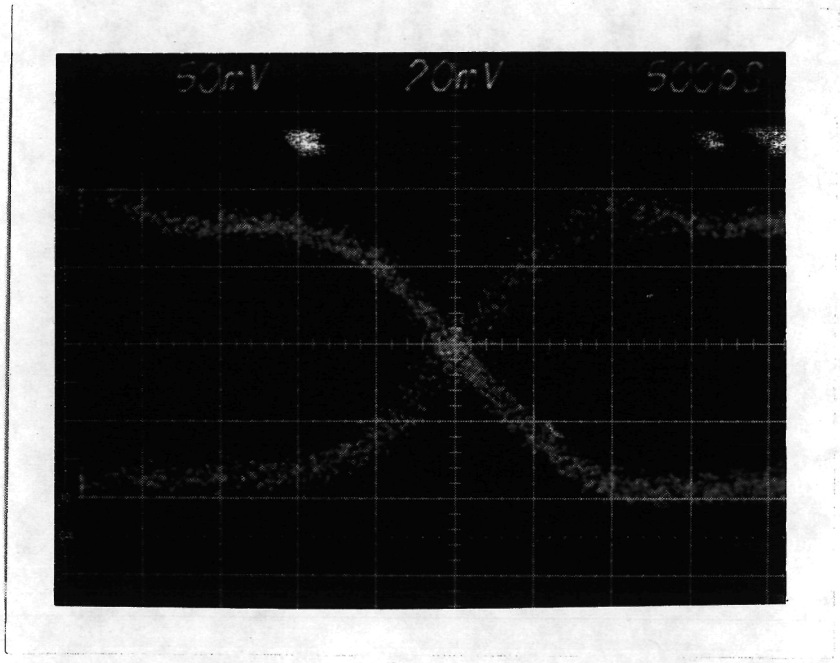


Figure 6-10. Demodulated QPSK Signal Eye Pattern

7. CONCLUSIONS AND RECOMMENDATIONS

The majority of the design goals of this contract were met. The direct modulation of the 60 GHz carrier using the quadriphase shift keying technique has been demonstrated. The exciter/modulator was built in millimeter integrated circuit to achieve small size and light weight. The results represent state-of-the-art performance in millimeter wave component and subsystem developments.

In the exciter development, a microstrip Gunn oscillator was phase-locked to a low frequency crystal reference source through a subharmonic mixer and loop electronics. An output power of +11 dBm was achieved at 60 GHz. The oscillator has a locking range extended from -180 MHz to +160 MHz and a capture range of ±10 MHz.

In the modulator development, a QPSK modulator was fabricated on sapphire substrate. The modulator consists of two 3-dB Wilkinson couplers, two microstrip-to-slotline transitions, and two biphase switches. The modulator was optimized to have 13 dB total insertion loss, ±3° phase error, and ±0.5 dB amplitude error.

The exciter and modulator were integrated with the data driver into a small housing measuring 1.8 x 2.5 x 0.9 in. The unit was fully characterized in meeting the performance goals.

Although most of the program goals have been achieved, several improvements are still required to further reduce the size and improve the performance. The following recommendations for future development are proposed to achieve these objectives.

1. The positions of the diodes are very critical in achieving good phase and amplitude balance. At 60 GHz, the beamlead package dimensions are 40% of a quarter wavelength. Slight offset of the diodes results in significant phase and amplitude imbalance. To mount the beamlead diodes in the right positions is a difficult and time-consuming task. To overcome this problem and improve the performance, we recommend the development of a monolithic chip with diodes grown in-situ. Since our QPSK modulator is built on sapphire substrate with a dielectric constant of 10,

which is close to that of GaAs, the same circuit design can be directly translated into the monolithic circuit on GaAs substrate.

2. No crosslink measurement and demodulation were conducted during this program. To use the QPSK exciter/modulator in communication systems, the development of a demodulator system and the analysis of crosslink are recommended.

3. The emphasis of this program was placed on the development of millimeter-wave hardware in the QPSK exciter/modulator. Little effort was directed at the reduction of size and weight of the phaselock electronics. The phaselock electronics were built using a crystal controlled reference oscillator and commercially available parts. To downsize the unit, it is recommended to miniaturize these eletronics by using a stable SAW oscillator as a reference source and hybridized electronics.

4. The 60 GHz Gunn VCO has a varactor tuning range of 0.5 GHz. Although this tuning range is adqequate for normal laboratory operation, it is desirable to have wider tuning range to avoid losing phaselock in a cold start.

5. The output port of the 60 GHz Gunn VCO is directly coupled to the QPSK modulator. No isolator or circulator was inserted to improve the isolation. The Gunn VCO is thus sensitive to the loading effects caused by the switching action of the modulator. Small variation of output power and frequency was observed due to the switching. To improve the performance, a low loss 60 GHz microstrip circulator is required and should be developed.

APPENDIX A: OPERATING MANUAL

1. TEST EQUIPMENT REQUIRED

   Power Supply +15 V @ 0.75 A

   Power Supply -12 V @ 0.5 A

   Power Supply +6.5 V @ 1.5 A

   Spectrum Analyzer (60 GHz)

   Power Meter (60 GHz)

   DC Voltmeter

2. TURN-ON/OFF PROCEDURE

2.1 Conditions

All power supplied should be turned on and the voltage adjusted to 0.0 V before connecting to the modulator/exciter.

2.2 Connect the spectrum analyzer and power meter as shown in Figure A-1.

2.3 Connect the power supplies as shown in Figure A-1.

2.4 Adjust the +15 V supply for +15 V ±0.1 V.

2.5 Adjust the -12 V supply for -12 V ±0.1 V.

2.6 Adjust the 6.5 V supply for +6.5 V ± 0.1 V.

2.7 The green lock light will be turned on as the Gunn supply voltage comes up, indicating the loop is locked.

2.8 "Turn Off" is accomplished by reversing the turn-on sequence.

3. CLOCK AND DATA INPUTS (Figure A-2)

Input	Connector	Level	Function
Clock 1	OSM	0 dBm	Clock to data drivers
Clock 2	OSM	0 dBm	
Data 1	OSSM	ECL	Data input (differentially driven)
Data 2	OSSM	ECL	

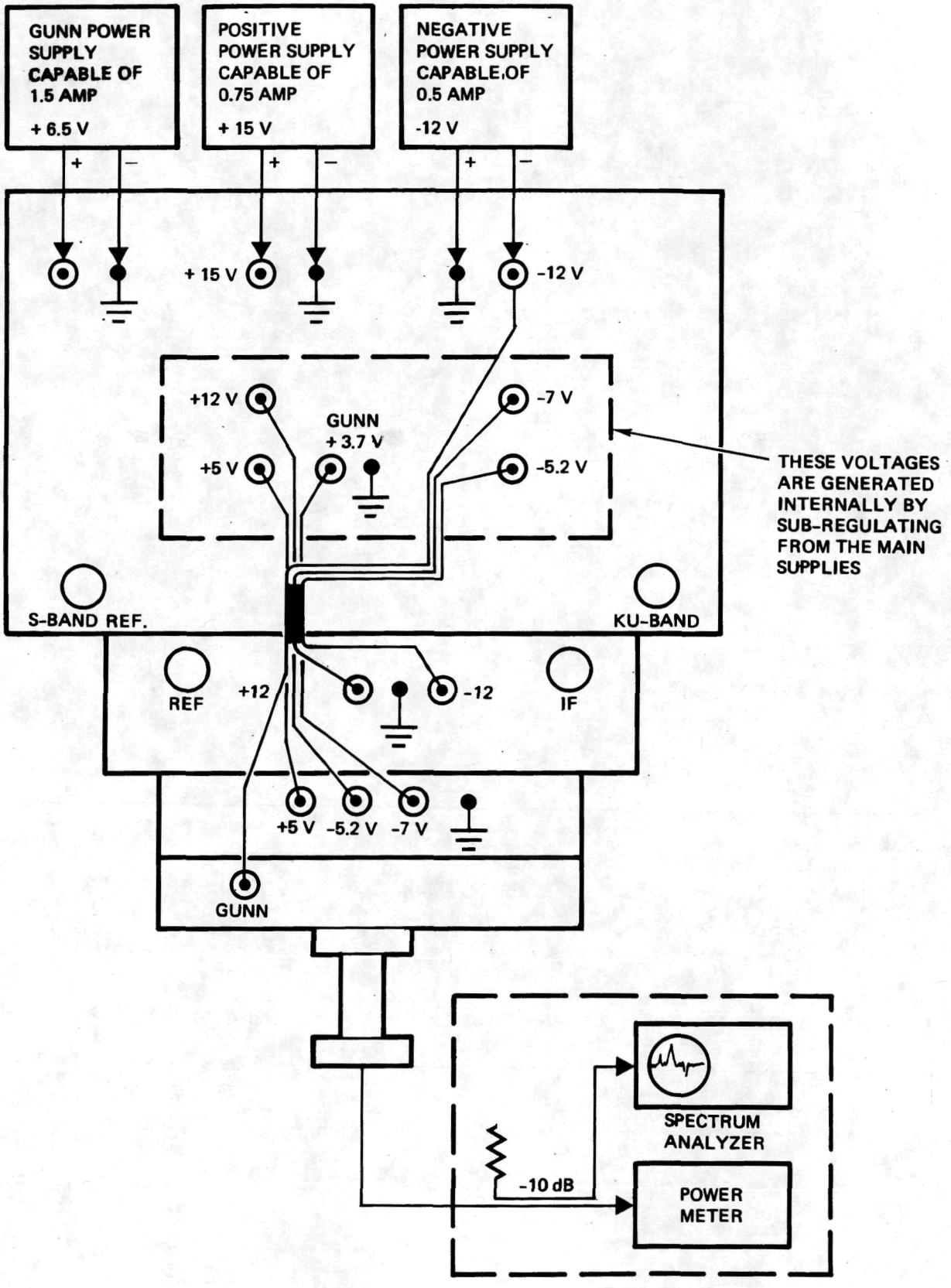


Figure A-1. Test Setup

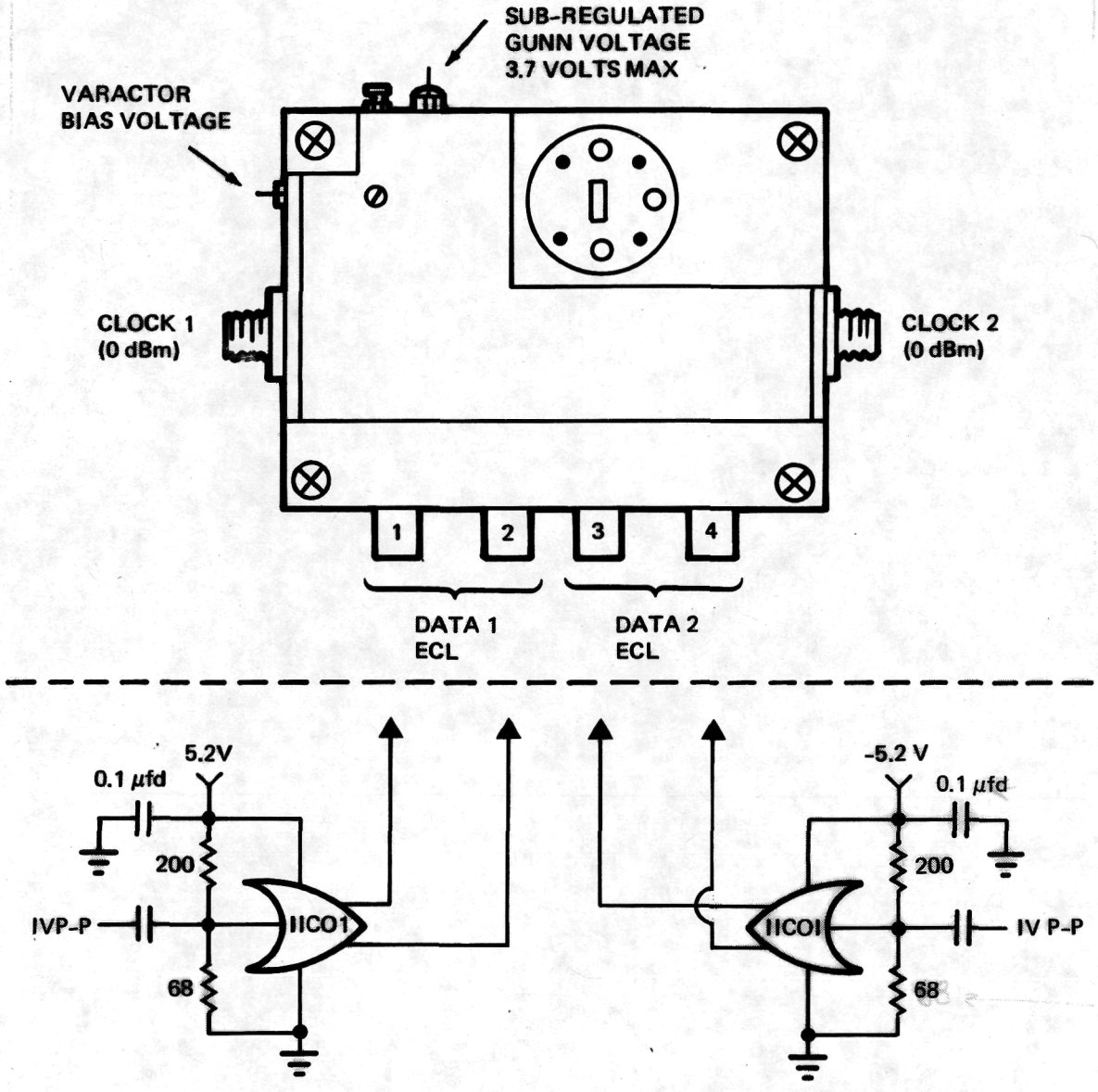


Figure A-2. Exciter/Modulator Module and Data Driver

4. TEST POINTS

A. Voltage: +15 V -12 V
+12 V - 7 V
+ 5 V -5.2 V

B. Lock: Indicates loop is locked when green light is on.

C. COS Ø Det.: Brings output of COS. Ø DET. out for test and adjustment.

5. ADJUSTMENTS

Adjustments are preset and <u>should not</u> require readjustment.

A. GUNN V-ADJ. - Adjusts the voltage to the Gunn diode (max. Gunn operating voltage = +3.7 V).

B. RAMP - Adjusts the ramp position.

C. VCO - Sets the varactor voltage.

D. COS. SEN. - Sets the threshold for lock indicator and ramp disable circuits.

E. SWEEP ON/OFF - Manually disables the ramp generator circuits for test and adjustment purposes.

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