



**Parametric Approach to Determining the  
Optimum Geometry for PZT MEMS Switches  
Intended for Digital Applications**

**by Robert Proie, Ronald Polcawich,  
Jeff Pulskamp, Daniel Judy, and Joe Qiu**

**ARL-TR-5404**

**December 2010**

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1. REPORT DATE (DD-MM-YYYY) December 2010		2. REPORT TYPE Summary		3. DATES COVERED (From - To) June to September 2009	
4. TITLE AND SUBTITLE Parametric Approach to Determining the Optimum Geometry for PZT MEMS Switches Intended for Digital Applications			5a. CONTRACT NUMBER		
			5b. GRANT NUMBER		
			5c. PROGRAM ELEMENT NUMBER		
6. AUTHOR(S) Robert Proie, Ronald Polcawich, Jeff Pulskamp, Daniel Judy, and Joe Qiu			5d. PROJECT NUMBER		
			5e. TASK NUMBER		
			5f. WORK UNIT NUMBER		
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) U.S. Army Research Laboratory ATTN: RDRL-SER-E 2800 Powder Mill Road Adelphi, MD 20783-1197			8. PERFORMING ORGANIZATION REPORT NUMBER ARL-TR-5404		
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)			10. SPONSOR/MONITOR'S ACRONYM(S)		
			11. SPONSOR/MONITOR'S REPORT NUMBER(S)		
12. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution unlimited.					
13. SUPPLEMENTARY NOTES					
14. ABSTRACT We designed lead zirconate titanate (PZT) microelectromechanical systems (MEMS) switches for low frequency digital logic applications. The devices were fabricated with a variety of design variables of interest, including actuator length/width, contact length, actuator/contact geometries, and contact metallurgy (Au/Pt, Au/Ru, and Au/Au). To assess the impact of each variable on device performance, we measured device wafers using a SUSS semi-automated probe station and associated control hardware and software, which evaluated contact resistance, actuation voltage, minimum actuation voltage using a constant bias voltage, and propagation delay. The measurements were then analyzed to determine the optimal switch geometry and contact material combination for digital applications. Future work is planned to examine repeatability of these statistics over multiple cycles and across multiple wafers.					
15. SUBJECT TERMS MEMs, mechanical logic, piezoelectric					
16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT UU	18. NUMBER OF PAGES 18	19a. NAME OF RESPONSIBLE PERSON Robert Proie
a. REPORT Unclassified	b. ABSTRACT Unclassified	c. THIS PAGE Unclassified			19b. TELEPHONE NUMBER (Include area code) (301) 394-1350

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## 1. Introduction/Background

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Using finite element analysis tools, such as ANSYS or CoventorWare, to estimate the behavior and performance of microelectromechanical system (MEMS) devices provides a great deal of useful performance predictions. These tools are capable of modeling extremely complex systems with a great degree of accuracy, assuming exactitude in the input describing that system.

Unfortunately, fabricated devices exhibit many characteristics—rounded edges, non-uniform deposition/etching rates, and residual stresses, many of which are specific to a given process flow—that are tremendously difficult to fully capture in these simulations (1). Therefore, it was important to study the impact of various device parameters on actual fabricated components.

MEMS switches are being examined for digital applications (2). A switch of this nature would provide the potential to integrate complex digital functionality into existing RF-MEMS phase shifter and actuator technologies, thus reducing cost and eliminating the need for multi-chip solutions. In addition, the extremely low power consumption and insensitivity to ion-based radiation would make the switch an ideal candidate for systems like unattended ground sensors. Work described in (2) illustrates an initial proof of concept, with switches intended for a similar purpose but designed at a much larger scale.

This recent effort required the switch have a high yield and low actuation voltage, while minimizing the area footprint. Leveraging the previous success of ohmic contact RF-MEMS switches (3, 4, 5), and 3-D scaling to achieve nanoscale switches (6), allowed for the production of designs with smaller, low-contact force switches. The process of verifying the functionality of these piezoelectric switches began with the layout creation for three basic designs. The switches, shown in figure 1, each have five key parametric properties in this study—actuator length and width, contact length, contact metallurgy, and the sacrificial layer used. Devices were fabricated in the Specialty Electronic Materials and Sensors Cleanroom facility at the Adelphi Laboratory Center (ALC). Afterwards, a semi-automatic testing system that used software algorithms specifically designed for these devices mapped the wafer and extracted many useful characteristics pertaining to switch performance.

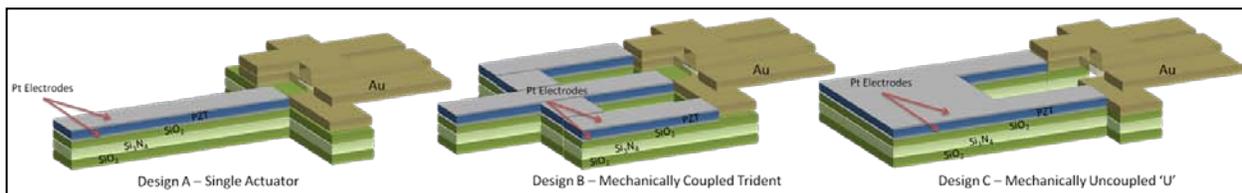


Figure 1. General structure of the three basic designs used in the parametric analysis.

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## 2. Switch Design Criteria

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The following metrics, in addition to high yield, describe the requirements for the switch. First, to reduce dynamic power consumption, the switch actuation voltage must not exceed an on-off delta voltage of 2 V. This requirement stems from the basic equation for dynamic power dissipation:

$$P = \frac{1}{2}C\Delta V^2f \quad (1)$$

In equation 1, P represents the dynamic power consumed, C is the capacitance of the structure,  $\Delta V$  is equal to the voltage change of the periodically cycled voltage, and f represents the frequency of operation. From this equation, there are three ways to minimize the power: reduce the frequency, shrink the size to effectively reduce the capacitance, or reduce the delta voltage. Since the power is proportional to the square of the voltage, small reductions represent large savings, which made it a focus of this work.

The next design criterion—minimizing the area footprint while maintaining process compatibility—translates into pushing the current lithographic techniques to the tolerance limits of the fabrication facility without introducing additional yield concerns. By reducing the size of the device, additional devices could occupy a given space on a wafer, enabling redundancy for a given operation. In addition, a smaller device translates directly into a smaller capacitance, reducing the overall dynamic power consumption. The capacitance also reduces the resistor-capacitor (RC) time constant directly affecting the switching speed.

The final design criterion—achieving a propagation delay of under 100 ns—ensures that the device operates with reasonable performance. Several factors play a role in achieving this metric with the maximum lower-to-upper contact gap and the capacitance charge-time associated with each switch dominating this benchmark. Those factors include the acceleration rate of the switch, and the consideration that switch bounce would occur during the initial contact each cycle. The latter concern can largely be addressed by controlling the actuation waveform, as discussed in (7).

Minimizing contact resistance was a secondary goal; the targeted contact resistance for these devices was approximately 1 k $\Omega$ .

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## 3. The Three Switch Designs

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All three of the switch designs share the same basic components. The switches are composed of a lower elastic layer containing a silicon dioxide (SiO<sub>2</sub>), silicon nitride (Si<sub>3</sub>N<sub>4</sub>) and SiO<sub>2</sub>, with

layer thicknesses previously stress-engineered to provide the residual stress that ensures that the actuator has a negative static deflection combined with a positive actuated deflection (3). On top of the elastic layer is a titanium/platinum layer, serving as the bottom electrode. Above that is the piezoelectric layer composed of thin-film lead zirconate titanate (PZT) with a zirconium (Zr)/titanium (Ti) ratio of 45/55, and then a top electrode of platinum. The electrical contacts for this system vary between gold (Au)-to-Au, Au-to-platinum (Pt) or Au-to-ruthenium (Ru).

In addition to sharing a fabrication stack, the basic operation of each switch, equivalent to a digital inverter or 2-to-1 multiplex gate, is the same. Each switch contains two contacts, one of which consists of an actuator-anchored cantilever that naturally rests on two gold traces attached to the substrate. This contact, termed a normally closed (NC) contact, shorts the two substrate traces together, provided that the potential difference between the two electrodes is small ( $\sim 0$  V). The other contact normally rests below two substrate-anchored parallel cantilevers. The application of a potential difference greater than the actuation voltage ( $V_{act}$ ) to the electrodes will deflect the switch upwards and short the two cantilevers together. This is termed the normally opened (NO) contact.

The three switches illustrated in figure 1 each contain various performance tradeoffs. Design 'A', which consists of a single rectangular actuator, presents the simplest and most traditional switch design included in this project. Many projects in the past, including a previous version of digital MEMS logic gates (2), used this design with success. There are, however, several inherent disadvantages. First, increasing the contact force for a given length actuator requires an increase in width. That increase translates into a larger capacitance and, thus, a slower switch that consumes more power. In addition, a wider switch requires additional time to fully release in the  $XeF_2$  etching step, which increases fabrication time and reduces the packing density. Figure 2 shows a fabricated device of this type.

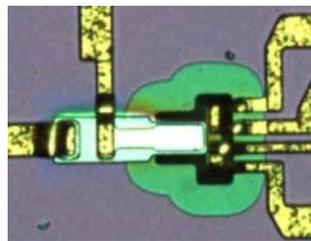


Figure 2. Fabricated design 'A' device.

The second design, which makes an effort here to minimize capacitance and the release time while effectively increasing the width of the device, takes a shape similar to a trident. Here, a narrow stem branches out into three rectangular sections that are rejoined at the end via the elastic layer. Thus, mechanical coupling exists between the three branches. This design should provide the greatest deflection for a given voltage, compared to designs 'A' and 'C', although

the added capacitance will negatively influence the speed. Figure 3 shows a fabricated device of this type.

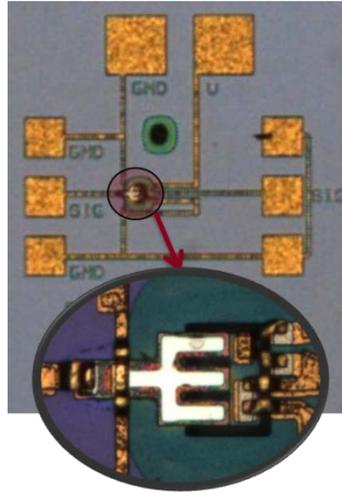


Figure 3. Fabricated design 'B' device.

Hybridizing the two previous approaches, design 'C' has the unique feature of two mechanically uncoupled branches. This allows the electrically unconnected branch to have more deflection freedom, while the other branch overcomes coulombic forces during a state change. This should provide a speed advantage over the other two designs, but it contains the added risk that electrical contact could form simultaneously at both contacts, thus potentially shorting power to ground in certain circuit designs. Figure 4 shows a fabricated device of this type.

Features of each of the three designs were varied parametrically across the wafer. The actuator lengths ranged from 3  $\mu\text{m}$  to 50  $\mu\text{m}$  and the widths varied on a design-by-design basis. Both 12  $\mu\text{m}$  and 25  $\mu\text{m}$  long cantilevers were used for contacts. The sacrificial layer used to make these contacts consisted of either photo-definable resist or evaporated silicon. Finally, fabrication included contact metallurgy combinations of Au-to-Au, Au-to-Pt, and Au-to-Ru.

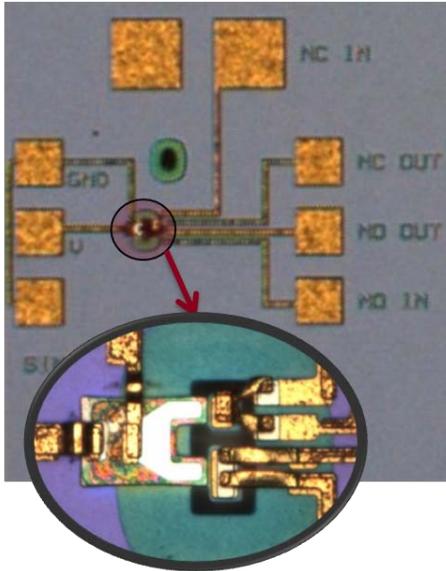


Figure 4. Fabricated design 'C' device.

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## 4. Experimental Setup

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Figure 5 shows the experimental setup used for this study. Either an Electroglas 2001X automated probe station or a SUSS PA200 semi-automated probe station served as the testing platform for these measurements. The experiment consists of two steps. First, a DC power supply drove the bias line of the device under test (DUT), with a voltage sweeping from 0 V to 15 V. During that time, a dedicated multimeter measured the voltage across an external load resistor. Based on known load, DC probe and cable resistances, and supply voltage, the testing software would extract  $V_{act}$  and the contact resistance ( $R_C$ ) as a function of bias voltage.

In the second step, an arbitrary waveform generator, set to produce a single square pulse, served as the bias source; additionally, a high speed, 2.5 GHz bandwidth, digital oscilloscope replaced the multimeter as the signal measurement tool. For each switch in that category, a square wave pulse with a high voltage equal to  $V_{act}$  drove the bias, and a 1 V DC signal drove one side of the contacts. The oscilloscope captured the output, and the testing software analyzed the data to determine the signal propagation time from bias application to output for the switch. This test only examined switches that achieved an electrical connection during step one.

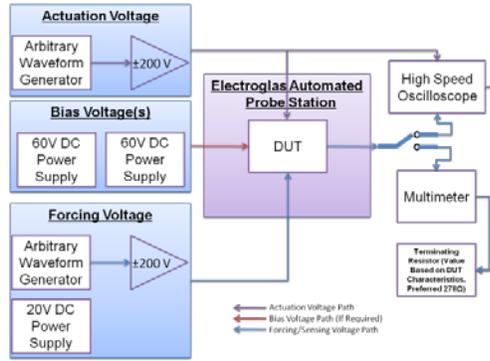


Figure 5. Experimental test setup to examine the performance of each device.

Note that a semi-automated SUSS probe station was sometimes used in place of the Electroglas probe station.

## 5. Results and Discussion

Initially, fabrication errors limited the success of the NC portion of the switches. The challenge has been overcome, and recent devices have demonstrated full functionality. All results presented here relate to the NO portion of the devices.

Figure 6 shows a summary of the results collected from a type ‘B’ device. The right image in figure 6 indicates a 2 V actuation voltage over three cycles, which shows a significant advantage that piezoelectric switches have over their electrostatic counterparts. At this voltage, it is feasible to envision complementary metal-oxide-semiconductor (CMOS) to MEMS logic communication busses without the need for digital-to-analog or analog-to-digital components on either side. A measurement of repeatability was performed to demonstrate consistency in pull in voltage and contact resistance.

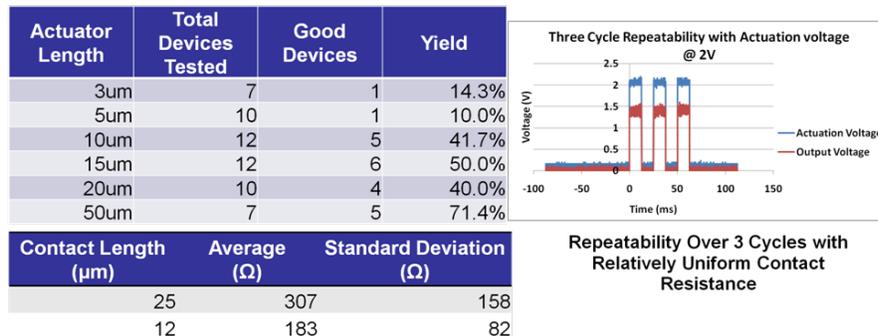


Figure 6. Results from one type ‘B’ device. The left table shows yield statistics and contact resistance based on actuator and contact dimensions, respectively. The right image shows three-cycle repeatability with an actuation voltage of 2 V.

Collected data indicates that the type ‘B’ design (see figure 3) produced the highest yielding devices. The yield of the type ‘C’ devices was lower on average, but comparable to type ‘B’ devices. For type ‘A’ devices, their best actuator length yields were under 10%. The investigation to determine the source of this significant degradation in functionality is ongoing, but current data suggests a strong relationship to the reduced contact force for these devices. In addition, many switches performed with a propagation time of under 100 ns (including the delays associated with the test setup), and several of the type ‘C’ devices performed in under 50 ns. Figure 7 shows a type ‘B’ device with a propagation time of ~99 ns and minimal bounce.

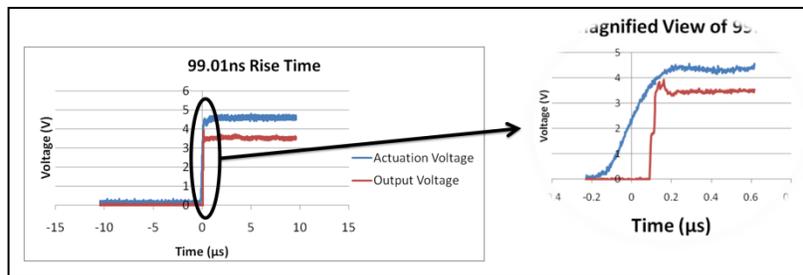


Figure 7. Signal propagation time under 100 ns.

Across all devices examined, the 25  $\mu\text{m}$  long contacts performed similarly to the 12  $\mu\text{m}$  variant, with 52% of the functional devices having 25  $\mu\text{m}$  contacts and 48% having 12  $\mu\text{m}$  contacts. When comparing the sacrificial layer used, however, this trend deviated. Devices using a photo-definable organic sacrificial layer performed much better with 25  $\mu\text{m}$  long contacts. Yield ratios of 3 to 1 in favor of 25  $\mu\text{m}$  long contacts were typical for a photoresist sacrificial layer. On the other hand, devices using a silicon sacrificial layer performed much better with the 12  $\mu\text{m}$  long contacts. Yield ratios of 17 to 3 in favor of 12  $\mu\text{m}$  long contacts were typical. The method of forming contact dimples with each sacrificial layer is a likely source for the observed yield variations.

In general, as the actuator length increased—up to 15  $\mu\text{m}$  in length—the yield would increase. Beyond 15  $\mu\text{m}$ , the percent yield would begin to level off. For these designs, shorter devices generate smaller contact forces, which would counter the advantages provided by the wider designs and lead to the lower recorded yields. These results were not conclusive, however, since fewer 3  $\mu\text{m}$  and 50  $\mu\text{m}$  long switches existed on each wafer compared to the 5  $\mu\text{m}$  through 20  $\mu\text{m}$  long switches.

Concerning contact metallurgy, the Au-to-Au combination produced stiction issues, an effect minimized by carefully monitoring  $V_{\text{act}}$  for each switch and preventing the application of higher bias voltages. Au-to-Pt and Au-to-Ru did not suffer from stiction issues.

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## 6. Summary and Conclusions

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A series of parametrically varied, thin-film PZT MEMS switches were successfully fabricated. Switches with a  $V_{act}$  equal to 2 V and a signal propagation time under 100 ns were successfully demonstrated. All of the switches were compared to a series of metrics to determine the optimal design parameters for digital applications. The highest yield for silicon sacrificial switches occurred with 12  $\mu\text{m}$  long contacts. For photo-definable organic sacrificial layer devices, the highest yields were observed with 25  $\mu\text{m}$  long contacts. Actuator length was observed to be directly proportional to yield up to 15  $\mu\text{m}$ , beyond which point no significant improvement was detected. Finally, contact metallurgy was seen to have a role in the occurrence of stiction, with the effect primarily occurring in Au-to-Au contacts.

Future work is intended to examine these designs across multiple wafers. In addition, studies to determine temperature impact and switch lifetime in  $\text{N}_2$  and in open atmosphere, and a further investigation into switching speed, are planned. These studies will aid in the demonstration of higher-level logic functions.

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## List of Symbols, Abbreviations, and Acronyms

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ALC	Adelphi Laboratory Center
Au	gold
CMOS	complementary metal-oxide-semiconductor
DUT	device under test
MEMS	microelectromechanical system
NC	normally closed
NO	normally opened
Pt	platinum
PZT	zirconate titanate
$R_c$	contact resistance
RC	resistor-capacitor
Ru	ruthenium
$\text{SiO}_2$	silicon dioxide
$\text{Si}_3\text{N}_4$	silicon nitride
Ti	titanium
Zr	zirconium

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